A Current Mirroring Integration Based Readout Circuit for High Performance Infrared FPA Applications

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***Abstract*—This paper reports a current mirroring integration (CMI) CMOS readout circuit for high-resolution infrared focal plane array (FPA) applications. The circuit uses a feedback structure with current mirrors to provide stable bias voltage across the photodetector diode, while mirroring the diode current to an integration capacitor. The integration capacitor can be placed outside of the unit pixel, reducing the pixel area and allowing to integrate the current on larger capacitance for larger charge storage capacity and dynamic range. The CMI unit cell allows almost rail-to-rail voltage swing on the integration capacitance for low voltage operation. The detector bias voltage can be adjusted independently for various detector requirements. By virtue of current feedback in the CMI structure, very low (ideally zero) input impedance is achieved. The unit-cell contains just nine MOS transistors and occupies 20 μm $\times$ 25 μm area in a 0.8-μm CMOS process. The CMI circuit provides a maximum charge storage capacity of 5.25×10^7 electrons and a maximum transimpedance of 6×10^7 Ω for a 5 V power supply and 2 pF off-pixel integration capacitance.**

***Index Terms*—Focal plane arrays (FPAs), hybrid readouts, infrared imagers, readout electronics.**

I. Introduction

Infrared focal plane arrays (FPA) have a wide range of military, medical, industrial, and scientific applications, where high resolution and high performance readout electronics is required. The resolution can be increased by increasing the number of pixels, but then, the pixel size needs to be reduced to decrease not only the overall chip area and therefore its cost, but also the cost of optics. However, the small pixel size limits the complexity, and hence the performance of the readout circuit. A high performance circuit should provide a stable and near zero detector bias to reduce the dark current and detector noise; it should have low input impedance to obtain high injection efficiency for integrating maximum amount of current generated by the detector on the integration capacitance and for increasing its bandwidth and decreasing its input referred noise; and it should have a large dynamic range to increase the maximum charge storage capacity, which requires large integration capacitance and high voltage swing on it [1]–[3]. The integration capacitor is preferred to be placed outside of the pixel to increase its value without increasing the pixel size.

Earlier readout structures, including self-integration (SI), source-follower-per-detector (SFD), and direct-injection (DI), are simple and occupy small area, but they cannot satisfy most of the high performance requirements [2]–[5]. Later amplifier structures, such as buffered-direct-injection (BDI) and capacitive feedback transimpedance amplifier (CTIA), provide a better performance in terms of injection efficiency and detector bias stability with the help of an in-pixel opamp [2]–[6], but their performance is limited with the quality of the opamp that should be implemented in a small pixel area. In addition, CTIA requires an in-pixel integration capacitor. A novel approach, buffered gate modulation input (BGMI) [7], provides in-pixel detector current amplification and background flux suppression and places the integration capacitance outside of the pixel, but it also requires in-pixel operational amplifier components for detector bias stabilization; therefore, it has area and op-amp dependent performance limitations. A recent novel approach, current mirroring direct injection (CMDI) [8], [9], satisfies the high injection efficiency and almost-zero detector bias requirements; however, the CMDI also requires the integration capacitor to be in the pixel, and therefore has large pixel area, low dynamic range, and low charge storage capacity. Another interesting approach, switched current integration (SCI) [10], provides large charge storage capacity with the use of an off-pixel integration capacitor; however, it requires an in-pixel amplifier that limits its detector bias and injection efficiency performance and affects the pixel area. In summary, all previous circuits have either low performance with simple structures, or high performance with large pixel area, due to their need for an in-pixel amplifier and/or an in-pixel capacitor.

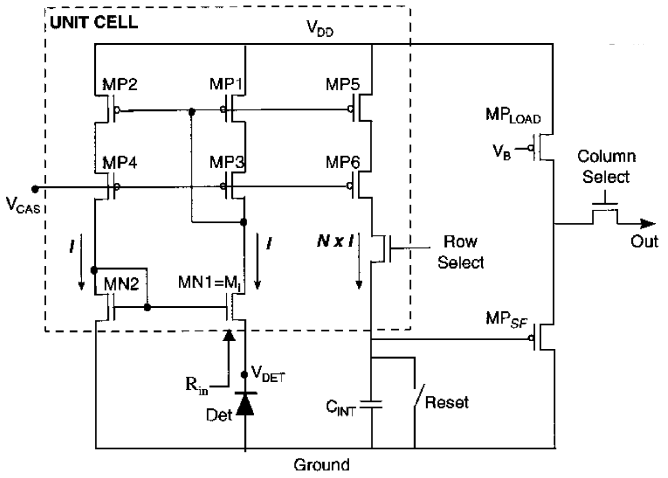

Fig. 1. Schematic view of the CMI preamplifier circuit, including the unit cell and off-pixel components.

This paper reports a new high performance readout structure, called current mirroring integration (CMI) [11], [12], which provides high performance without needing an in-pixel opamp or integration capacitor. The CMI preamplifier circuit combines the benefits of the CMDI and SCI circuits, while eliminating their drawbacks, to achieve a high performance preamplifier in a small size. Contrary to SCI, the CMI circuit provides high injection efficiency and stable and almost-zero detector bias without a need for the in-pixel amplifier; and contrary to CMDI, it is implemented in a small pixel area with only nine transistors in the unit cell and without an in-pixel capacitor and can provide high charge storage capacity and high dynamic range with the use of large off-pixel integration capacitance. In addition, it has rail-to-rail operation with its new structure and with the use of high-swing cascode current mirrors. The CMI circuit can be used not only with photovoltaic detectors that require stable zero detector bias, but also with photoconductive detectors, such as quantum-well infrared photodetector (QWIP) detectors that require a certain, stable bias voltage larger than zero. The stable, near zero detector bias in a photovoltaic detector allows reducing the dark current and noise of the detector.

II. Circuit Structure

Fig. 1 shows the schematic view of the CMI preamplifier circuit [11]. The unit cell is very simple and requires only nine transistors,

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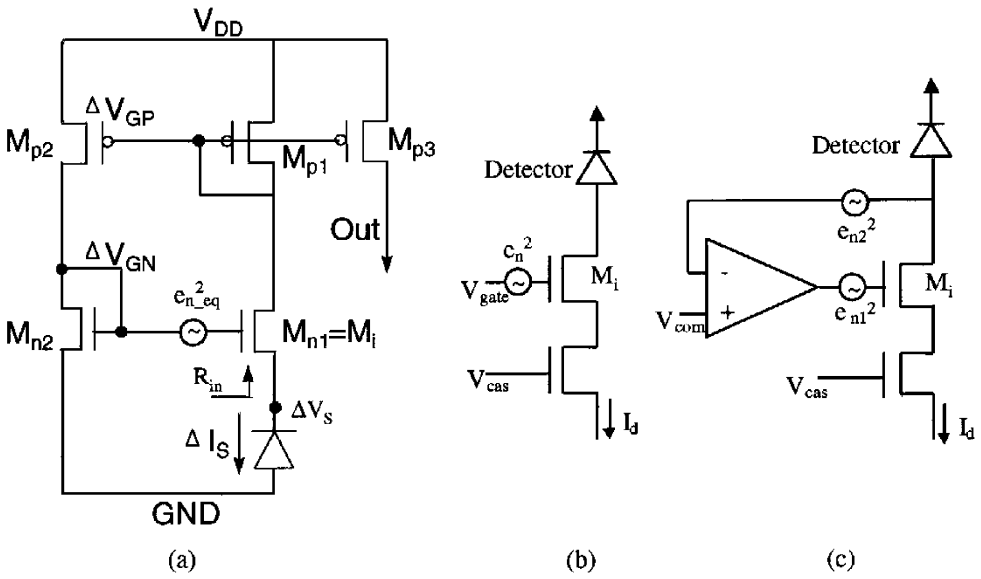


Fig. 2. Simplified schematic view of various preamplifier structures used for analytical calculations and noise comparisons: (a) CMI, (b) DI, and (c) BDI structures.

and the rest of the circuit components are placed outside the pixel area, including the integration capacitance, the source follower, and the detector diode, which is usually hybrid connected to the circuit.

The circuit operation is very simple: infrared radiation induces a current in the detector diode, and this current passes through MN1 and is mirrored to MN2 using the high-swing cascode current mirror formed with transistors MP1-MP4. Since MN1 and MN2 are also connected as a current mirror, their gate-to-source voltages are forced to be equal, resulting in an almost-zero detector bias [8], [9]. This structure also results in low input impedance, and therefore, most of the induced detector current is injected to the readout circuit even in the cases where the detector resistance is low. The induced detector current is also copied and transferred to the external integration capacitance using the transistors MP5 and MP6, whose sizes can be adjusted to provide a gain, N, on the mirrored current, increasing the sensitivity and signal-to-noise ratio (SNR). The row select transistor provides the selection of rows in a consecutive manner, and hence, enables electronic scanning.

The voltage obtained at the capacitance node swings from 0 V to almost $V_{\rm DD}$, i.e., the circuit allows rail-to-rail operation, providing high dynamic range. The capacitor voltage is buffered with a pMOS source-follower buffer, which inherently decreases the voltage swing due to threshold voltage and reduces the linearity of the signal, however, these effects can be eliminated by using either higher positive voltage supply for the source-follower buffer or other high swing buffer structures. Each unit cell requires four input signals, including $V_{\rm DD}$, ground, row select, and bias voltage for cascode structures. The number of input signals to each unit cell can be reduced to three with the use of more advanced current mirrors, such as high swing self cascoded current mirrors [12]–[15].

The array implementation of the CMI circuit can be achieved using the approach of the SCI [10]. The buffer is shared by all pixels of one column together with one big integration capacitance, which is placed outside the unit cell unless otherwise is required by the specific application. The buffer output is transferred to the signal processing unit, which is selected as a correlated double sampling (CDS) circuit to improve the noise performance of the overall system by reducing the fixed-pattern-noise (FPN) and $1/f$ noise considerably. Although complementary source follower buffers in the CDS circuit further reduces the swing observed at the output node, this simple structure is selected to demonstrate the operation of the CMI.

III. Circuit Performance

The high performance of the CMI circuit has been verified by both analytical calculations and detailed simulations. Table I shows the comparison between CMI and other unit cells in terms of input impedance, detector bias control, pixel area, and noise performance. The CMI structure has a very good performance in each of these parameters, comparable to or better than the other structures. Fig. 2 shows the simplified structures view of various preamplifier structures used for analytical calculations and noise comparisons.

The detector bias in the CMI structure is similar to the CMDI structure [8] and can be expressed as

$$V_{\rm DET} = \frac{K_P}{K_N} \times \Delta V_{\rm TP} + \Delta V_{\rm TN} \tag{1}$$

where K_N and K_P are the geometry constants of the nMOS transistors and pMOS transistors, respectively; and $\Delta V_{\rm TN}$ and $\Delta V_{\rm TP}$ are the mismatch values of the threshold voltages of the nMOS transistors and pMOS transistors, respectively. As $\Delta V_{\rm TN}$ and $\Delta V_{\rm TP}$ are very small within each pixel, the detector bias is very stable and close to zero, minimizing dark current and detector noise. It should be noted in here that these results are also valid for different detector bias voltages. The CMI circuit can be used for some applications requiring a nonzero detector bias point, e.g., photoconductive QWIP detectors, by changing the ground potential in the current mirror structure to the required bias voltage value up to 3.8 V, without affecting the overall circuit performance and bias stability.

Another advantage of the CMI structure is that the input resistance seen by the detector is ideally zero. This is important to obtain high injection efficiency, which is defined as the ratio of current delivered to the preamplifier to the overall photodetector current (i.e., $R_D/(R_{\rm in} + R_D)$, where R_D is the detector resistance and $R_{\rm in}$ is the input resistance of the readout circuit). The effective input resistance of the readout preamplifiers based on current feedback structures, such as

TABLE I
COMPARISON BETWEEN COMMON UNIT CELL STRUCTURES AND CMI. THE CMI STRUCTURE PROVIDES EITHER COMPARABLE OR BETTER PERFORMANCE THAN THE OTHER STRUCTURES IN ALL PERFORMANCE PARAMETERS, AS LONG AS γ IS MADE CLOSE TO 1

Structure	*Readout Input Impedance*	*Detector Bias Control*	*Pixel Area*	*Input Referred Noise*
DI	$\frac{1}{g_{mi}}$	Not stable. Changes during integration	Small	$\frac{e_n^2}{\left(R_D+1/g_{mi}\right)^2}$
GMI	$\frac{1}{g_{mi}}$	Not stable. changes during integration	Small	$\frac{2e_n^2}{\left(R_D+1/g_{mi}\right)^2}$
BDI	$\frac{1}{g_{mi}\times(1+A)}$	Stable. Controlled by an OpAmp Feedback	Large, in-pixel op-amp and integration capacitor	$\frac{e_{n1}^2}{\left(R_D+1/g_{mi}\right)^2}$
CTIA	Amplifier input impedance	Stable. Controlled by an OpAmp Feedback	Large, in-pixel op-amp and integration capacitor	$e_{n\,amp}^2\frac{(C_{fb}+C_{\det})^2}{A^2\times C_{fb}^2}$
SCI	$\frac{1}{g_{mi}\times(1+A)}$	Stable. Controlled by an OpAmp Feedback	Moderate, no in-pixel capacitance, but in-pixel op-amp components	$\frac{e_{n1}^2}{\left(R_D(1+A)+1/g_{mi}\right)^2}$
BGMI	$\frac{1}{g_{mi}\times(1+A)}$	Stable. Controlled by an OpAmp Feedback	Moderate, no in-pixel capacitance, but in-pixel op-amp components	$\frac{e_{n1}^2}{\left(R_D(1+A)+1/g_{mi}\right)^2}$
CMDI	$\frac{1-\gamma}{g_{mN2}}$	Stable and very close to zero. Controlled by a double current mirror feedback	Large due to in-pixel capacitance	$\approx g_{mi}^2 e_{n\_eq}^2$
CMI	$\frac{1-\gamma}{g_{mN2}}$	Stable and very close to zero. Controlled by a double current mirror feedback structure	Small, requires 9 transistors in-pixel, but uses off-pixel integration capacitance	$\approx g_{mi}^2 e_{n\_eq}^2$

∗A: Amplifier; $\boldsymbol{\gamma}$: : parameter defined in (4); $\boldsymbol{g}_{mi}$: Input transistor; $\boldsymbol{R}_D$: detector resistance; $\boldsymbol{C}_{\rm fb}$: CTIA feedback capacitance; and $\boldsymbol{C}_{\rm det}$: detector capacitance

CMI and CMDI, can be found by calculating the current change ΔI_S due to the voltage change ΔV_S [8], [9], as

$$R_{\rm in}=\frac{\Delta V_S}{-\Delta I_S}=\frac{1-\gamma}{g_{mN2}} \tag{2}$$

where γ is defined in terms of transistors transconductaces as

$$\gamma=\frac{g_{mP1}}{g_{mP2}}\times\frac{g_{mN2}}{g_{mN1}}. \tag{3}$$

Equation (2) shows that, by perfect matching of copying transistors, a near-zero input impedance, and hence, unity injection efficiency can be achieved. Although a perfect matching is practically impossible, γ can be made very close to unity by using proper design and layout techniques. For example, for a γ of 99.6% and a typical g_{mN2} of 2 μA/V, $R_{\rm in}$ can be reduced to a value as low as 2 kΩ, providing a very low input impedance for high injection efficiency for even low resistance infrared detectors. In fact, it is reported [9] that the injection efficiency in these type of current feedback structures can even provide an injection efficiency higher than 100% by making γ larger than one, and therefore $R_{\rm in}$ negative resistance. However, care should be taken to prevent oscillation of the circuit when operating in this mode.

It should be noted here that short channel effects are not considered in these calculations, and therefore, it is assumed that the variations in the currents through MP1 and MP2 are only due to transistor mismatches. However, short channel effects can cause large variations in the currents and transistor g_m values, degrading the performance of the circuit. This problem is solved in a great extent in CMI with the use of the high-swing cascode current mirror on the pMOS stage, as verified with detailed simulations and fabricated circuits. A cascode is added to the current mirror mainly to improve the linearity of current transfer at the output. A high swing self-cascoding topology is used [13]. A by-product of the cascode in the CMI loop is further reduction in the input impedance owing to improved current loop gain.

Input referred noise of the CMI circuit is also comparable to the other structures, mainly due to the fact that its input impedance is very low.

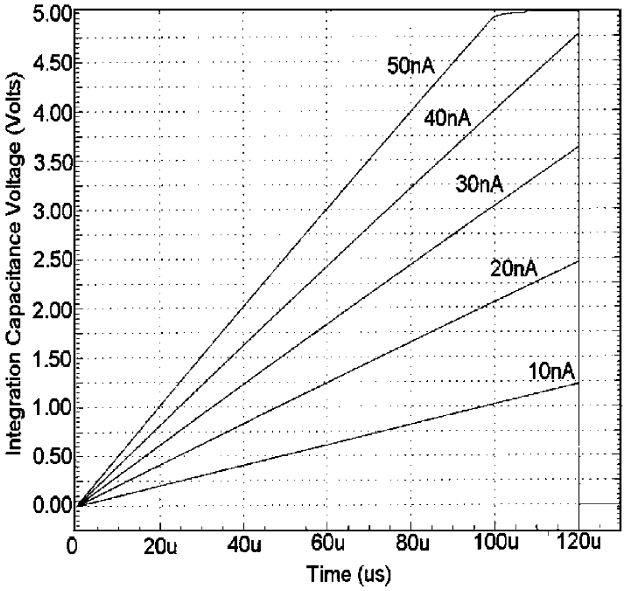


Fig. 3. Simulation results of the CMI circuit. The waveform shows the integration curves for various current values, verifying the high linearity and high output voltage swing. Here, the integration capacitance is chosen as 1 pF to show the dynamic range.

The input referred noise is directly related with the input impedance of the readout electronics and can be represented in a general form as [16]

$$i_n^2 \sim g_{\rm mi}^2 e_n^2 \left(\frac{R_{\rm in}+R_D}{R_D}\right)^2 \tag{4}$$

where $g_{\rm mi}$ is the transconductance of the injection transistor, e_n^2 is the equivalent voltage noise source at the input injection transistor, R_D is the detector resistance, and $R_{\rm in}$ is the preamplifier input resistance seen by the detector. Fig. 2 shows circuits used to compare the noise CMI with noise of DI and BDI structures [16], and Table I summarizes the overall noise values of various preamplifier structures. The total equivalent noise of the CMI circuit at the input transistor is large due to current mirrors, and it can be modeled as

$$e_{n-eq}^2 = e_{n-n1}^2 + e_{n-n2}^2 + \left(\frac{g_{mp1}^2}{g_{mn1}^2}\right)\left(e_{n-p1}^2 + e_{n-p2}^2 + e_{n-p3}^2\right) \tag{5}$$

considering the noise contributions of the each transistor in the simplified model. However, main advantage of the CMI structure is that it is possible to achieve low input impedance in a small pixel area. For example, when γ is equal to a moderate value of 0.99, it improves the input resistance by a factor of 100. The same effect is observed in BDI and SCI structures when the gain, A, of the amplifier is 100. However, it is difficult to obtain this gain in a small area, which forces the amplifier to be implemented as a simple operational transconductance amplifier (OTA) with small gain. Placement of an amplifier in each pixel also increases the power dissipation of the BDI and SCI structures. Therefore, CMI provides a very low input impedance and a moderate input referred noise.

The CMI has also a number of advantages compared to the CMDI structure. First of all, γ is made closer to one in CMI structure compared to CMDI structure since channel length effects on the current mirrors are reduced with the use of high-swing cascode current mirrors. Besides, the integration capacitor in the CMDI structure is inside the unit cell; therefore, a large pixel area is required to have a high charge storage capacity and high dynamic range. Also,

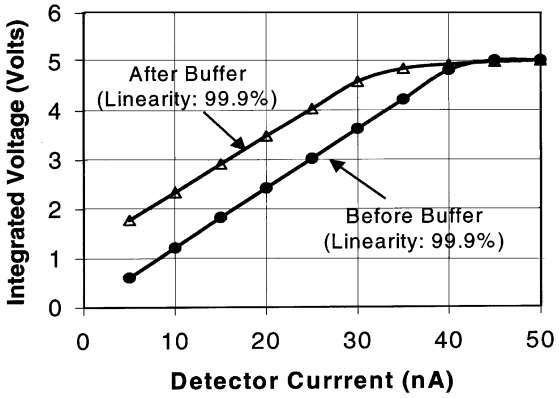


Fig. 4. Integrated voltage values obtained for different detector currents both before and after the source follower buffer, while the integration time is fixed at 120 μs. These results show that the CMI circuit provides linearity better than 99% for a output voltage swing between 0 and 4.5 V before and after the source follower buffer.

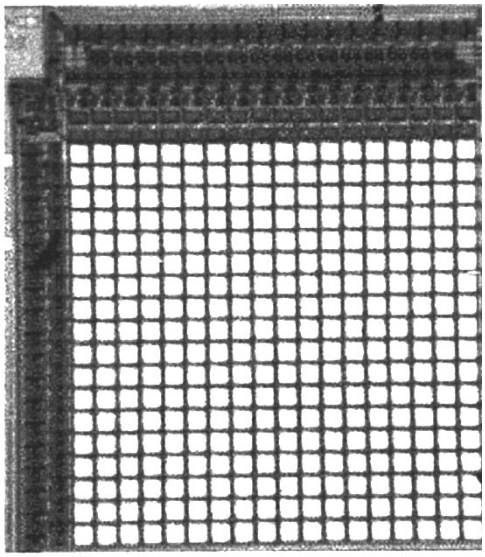
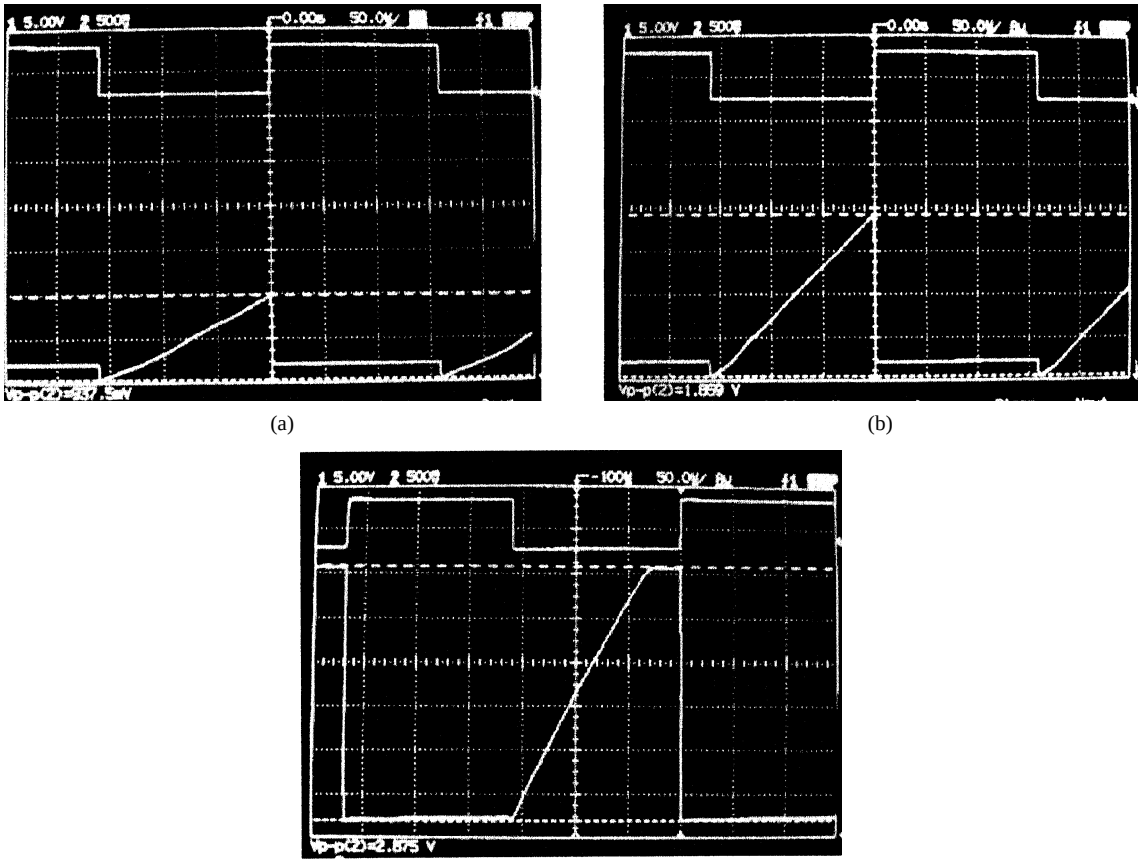


Fig. 5. SEM photograph of fabricated 16×16 CMI readout array implemented in a 0.8-μm CMOS technology.

CMDI has a limited voltage swing on the integration capacitance, while CMI can integrate a voltage on the integration capacitance from ground to almost $V_{\rm DD}$. Fig. 3 shows CMI integrated voltage levels at the capacitance node for current values between 10 and 50 nA for a 1-pF capacitance, verifying the high linearity and almost rail-to-rail output voltage swing of the CMI circuit. Fig. 4 shows the integrated voltage values for different detector currents both before and after the source follower buffer. According to this figure, CMI provides a linearity better than 99% for an output swing between 0 and 4.5 V before and after the source follower buffer. It can be seen that the buffer slightly degrades the linearity and decreases the value down to 96% for an output voltage swing larger than 4.5 V. The integration time is set as 120 μs for these simulations, but it can be reduced for large format FPAs, such as 640×480.

CMI also provides much higher charge storage capacity and dynamic range compared to CMDI, both due to higher voltage swing on the integration capacitance and due to fact that the integration capacitor can be selected to be large, as it does not have to be inside the unit cell. The maximum charge storage capacity for CMI is calculated as 5.25×10^7 electrons for 2 pF integration capacitance using 5 V supply,



(a) (b)

(c)

Fig. 6. Measurement results of the CMI unit cell with simple source follower buffers for different detector current values: (a) 20 nA, (b) 40 nA, and (c) 70 nA, while the integration time is fixed at 120 μs.

and it can be further increased by increasing the off-pixel integration capacitance or the supply voltage. It should also be mentioned here that only simulation results of the CMDI unit cell has been presented in the literature [8], [9], while CMI has been fabricated and tested not only in a unit cell format but also in an array format.

IV. Implementation and Test Results

A CMI readout test chip was designed in a 0.8-μm CMOS process to verify its operation. The chip includes the CMI unit cell and a fully functional and operational 16×16 prototype array. Fig. 5 shows an SEM view of fabricated 16×16 CMI readout array. Fig. 6 shows the test results of the CMI unit cell for different current values for a 120-μs integration interval. In Fig. 6(a), the integration capacitance is integrated up to approximately 1 V for a detector current of 20 nA. When the integration current is doubled, the capacitance voltage at the end of integration time is also doubled as shown in Fig. 6(b). The capacitance is saturated around 2.9 V for current values larger than 50 nA; for example, Fig. 6(c) shows the saturated integration curve for an integration current of 70 nA, where the swing is between 1.2 and 4.1 V. Fig. 7 shows the linearity measurement results of the fabricated CMI unit cell for different current values ranging from 10 to 50 nA for a 120-μs integration interval. As can be noticed from the figure, the CMI structures provides better than 99% linearity in the obtained voltage swing, i.e., 2.8 V. Table II summarizes the performance parameters of the CMI structure.

It should be noted here that the measured voltage swing at the output is smaller than rail-to-rail voltage swing due to the threshold voltage

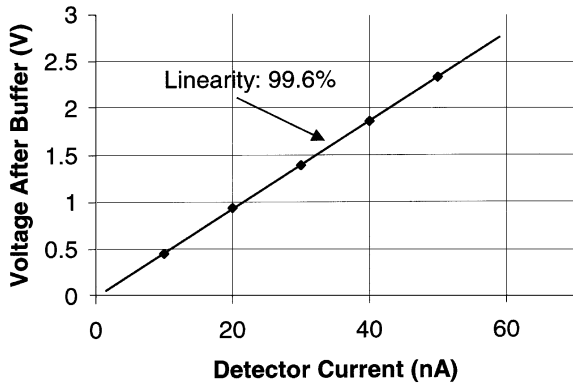


Fig. 7. Measurement results of the fabricated CMI unit cell, verifying its functionality and linearity.

drops in the source follower buffer circuits, as explained before. In fact the CMI unit cell can provide a very high output voltage swing (almost rail-to-rail), and this can be utilized by using high-swing operational amplifier structures as buffer circuits. The use of an operational amplifier as a buffer will also improve the linearity of integration curves after the buffer structure. Deviations from linearity in the integration apparent at the beginning of each integration interval are due to transients in the voltage buffer providing the measurement. These transients do not affect the final observation of the integration value itself. These measured responses also verify the operation and the linearity of the CMI structure.

TABLE II
SUMMARY OF THE PERFORMANCE PARAMETERS OF THE CMI UNIT CELL

Parameter	Results
Injection Efficiency	~100%
Integration Voltage Linearity	>99%
Integration Voltage Swing	Almost rail-to-rail
Transimpedance	$6x10^7\ \Omega$
Maximum Charge Capacity	$5.25x10^7$ electrons
Input Impedance ($I_{DETECTOR}$=50nA)	2.7 kΩ
Controllable DC Bias Range	0V-3.8V
Pixel cutoff frequency (R_{det}=250K, C_{det}=100fF)	>2MHz
Power Dissipation (in the current design N=2)	$(2+N)xI_{DETECTOR}xV_{DD}$
Power Supply	0-5V
Circuit Size	$20x25\mu m^2$
Pixel Pitch	$50x50\mu m^2$
Technology	0.8 μm CMOS

V. CONCLUSION

A new readout structure called CMI is designed for high resolution and high performance infrared FPA applications. This circuit provides almost 100% injection efficiency, almost-zero detector bias, large output voltage swing, very high linearity, and very good noise performance, while it can be implemented in a small area. The charge storage capacity of the circuit is calculated as 5.25×10^7 electrons for a 2-pF integration capacitance and a 5-V supply. Since the integration capacitor is placed outside of the pixel, the charge storage can be increased by simply increasing the value of the integration capacitance. The circuit provides a transimpedance of $6 \times 10^7\ \Omega$ for the same capacitance and power supply values. The CMI unit-cell employs only nine MOS transistors and occupies an area of 20 μm$\times$25 μm in a 0.8-μm CMOS process. The functionality of the CMI was verified through measurements on the fabricated test chip. The CMI readout circuit can be used not only in advanced high performance and high resolution infrared imaging applications, but also in other high performance imaging applications such as CMOS imagers operating in the visual spectrum.

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