On-Chip Self-Calibration of RF Circuits Using Specification-Driven Built-In Self Test (S-BIST)

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Abstract

In the nanometer design regime, analog and RF circuits are expected to be increasingly susceptible to process, noise and thermal variations. Shifting threshold voltages on the NMOS and PMOS devices of a mixer, LNA or power amplifier, for example, can affect the design specifications of such circuits (such as gain). Thermal variations can affect carrier mobilities of NMOS and PMOS devices differently, further affecting circuit performance. To solve these problems, a new self-calibration approach driven by a Specification-driven Built-In Self-Test procedure (S-BIST) is proposed. This S-BIST procedure uses alternate specification test techniques to predict the performance specifications of the circuit-under-test from the S-BIST response. The results of the S-BIST procedure are used to change the operating point of the circuit to maximally compensate the analog/RF circuit for loss of performance. The proposed S-BIST approach has been applied to a 2.4GHz low noise amplifier and performs well in the presence of temperature and process variations.

1. Introduction

Future CMOS technologies (sub-90nm) will integrate complex RF/analog/digital circuits on-chip. A key cause of concern is the effect of process variations on the performance of analog/RF circuits resulting in loss of manufacturing yield. In addition, these circuits have to function reliably under adverse field conditions (thermal, noise and battery power conditions).

This paper is concerned with on-chip self-calibration techniques for RF circuits to make them immune to thermal (in the field) and process (during manufacturing) variations. In the past, such calibration has been difficult due to the inability to measure deviations of RF circuit specifications from the expected, using on-chip mechanisms. While it is possible to test whether a circuit meets all its design specifications using complex external test instrumentation (RF stimulus generators, high-frequency RF measurement devices), it is not possible to measure all the design specifications of an RF circuit on-chip easily for self-calibration. Current RF built-in self-test (BIST) techniques target one or a few RF design specifications and are difficult to implement on-chip. Further, self-calibration requires the ability to perform circuit diagnosis from the test results. Once the cause of the performance loss is determined, necessary action can be taken to compensate for the cause (thermal, process variations, degradation due to electromigration/hot-carrier effects/aging).

In this paper, we propose a new self calibration technique based on a *built-in alternate test methodology*. The procedure (called the S-BIST procedure) consists of running a *built-in alternate test* [7-12] on the RF circuit to determine its performance specification values accurately. In order to determine *how* to change the control parameters, it is necessary to first know *which* of the circuit specifications have been affected by the changed environment and by *how much*. Built-in alternate test provides such information for self-calibration. Then corrective action is taken by *adapting* the bias voltages/currents of the RF circuit to the changed environment or process variations using a *self-calibration* procedure. This is possible due to the fact that most Systems-on-Chips (SoCs) have an associated on-board DSP processor to process circuit data and serve as the interface between the circuits and the external world. The DSP processor allows implementation of a digital closed-loop compensation control algorithm that allows *optimal self-calibration* of the RF circuits involved. The specific effects that we wish to detect and protect the circuits against are the following:

1. Thermal effects: Large temperature swings affect RF device bias current changes, thereby amplifying mismatch effects and degrading performance.
2. Process variation effects: In the deep submicron regime, process variations are expected to be significant and can cause performance loss due to threshold voltage mismatch, etc.

In the following, prior work is discussed followed by a discussion of the alternate test methodology. The

proposed S-BIST driven self-calibration methodology is then described. Simulation results for a self-calibrating low-noise amplifier (LNA) designed with 0.18μm CMOS rule set are presented.

2. Previous Work

Various methods for reducing circuit performance variations are available in the literature. For example, self-calibration techniques are an integral part of analog-to-digital and digital-to-analog converter designs [1][2], which trim reference voltages or capacitances to reduce device mismatch. However, these approaches have limitations in RF circuit applications. On the other hand, alternative solutions have been proposed which are inherently robust. One such example is the use of bandgap references [3] which provide bias voltages immune to temperature variation. Similarly, circuitry proposed in [4] compensates for the mismatch of current mirrors, whereas the feedback circuit in [5] tracks predefined process variation related effects such as transistor thresholds, body effect, and channel length modulation. In addition, predistortion linearization has been recently employed as a common technique for RF power amplifiers [6]. This compensates for the presence of nonlinearities by applying predistorted input signals.

The above techniques [1-6] are designed only to tackle specific factors such as temperature, selected process variations or a single performance specification. In addition, they are application specific and require significant increase in design time to incorporate self-calibration. Moreover, the range of performance variation over which compensation can be performed is limited by the fact that the compensation circuitry is itself exposed to the same environmental conditions as the test circuitry itself. In this paper, we propose a universal RF self-calibration scheme to compensate circuits for temperature and/or process variations. The performance evaluation scheme is specification centric so that the deviations are compensated only when they affect the end specifications. In addition, the *compensation is performed via digital algorithms* that are "immune" to thermal and process effects.

3. Built-In Alternate Test

In the S-BIST approach, first an *alternate test* [7-9] is applied to the circuit under test. The benefit of using an alternate test is that all the RF circuit's performance specification values can be predicted accurately from the observed test response. There has been significant work in the past on applying alternate test ideas to analog, mixed-signal and RF circuits. The overall alternate test scheme is depicted in Figure 1.

A specially crafted test stimulus is applied to the DUT, and is selected so that the test response is *strongly correlated to all the specifications of interest*. A nonlinear (regression-based, obtained through a calibration procedure) mapping function provides the relationship between the test response and the specifications of interest. Thus, the DUT specifications can be predicted accurately from the alternate test response. The predicted DUT specification values are used to make pass/fail decisions.

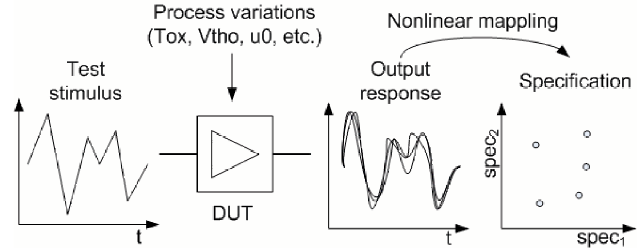


Figure 1. Alternate test methodology.

In the past, alternate tests have been geared towards production test time and test equipment cost reduction. The use of alternate tests for self-calibration has additional key requirements: 1) the RF test stimulus must be generated on-chip using available test resources, 2) the available on-board or embedded ADCs must be able to capture the alternate test response, 3) the response capture and analysis/feedback scheme for self-calibration must be immune to thermal/process variations.

The RF built-in alternate test schemes proposed in [10-12] already address some of these challenges. For production test of RF circuits, alternate tests consist of single sinusoids or multitone stimulus easily implemented on-board or on-chip. Furthermore, these utilize RMS/peak/envelope detectors (called "feature extractors") to extract DC or low frequency signal components from the RF output response. These *response features* enable the use of on-chip/on-board ADCs already available in the system. In addition, by using these feature extractors, it is possible to compensate for thermal and process variation induced errors in the response circuitry. In the temperature compensated configuration [10], feature extractors are directly connected to the test stimulus generator as well as the LNA output. Consequently, the regression model that maps the alternate test response to the test specification values of the DUT, along with the data from the feature extractors connected directly to the test stimulus, can be calibrated to compensate for thermal swings. In the literature, RF built-in alternate tests have been reported where the test specification value prediction error is the range of ±0.2% to ±5%.

The S-BIST methodology for self-calibration involves the use of alternate BIST techniques for RF components such as mixers, LNAs and RF power amplifiers. These are based on the principles described above, using a) carefully

crafted test stimuli that are possible to generate on-board/chip, b) carefully selected test response feature extractors that are immune to thermal and process variations, and c) use of an embedded DSP processor for completely autonomous test response analysis and self calibration.

4. S-BIST Driven Self-Calibration

The proposed S-BIST driven self calibration technique is designed to compensate for circuit performance degradation due to temperature and process deviations from the nominal. Process variations such as the shift of threshold voltage, oxide thickness and geometric size of a transistor directly affect the circuit performance. For example, threshold voltage shift affects transistor bias current and hence, its transconductance. In terms of temperature, although commercial analog and microwave electronics typically work over a range of 0°C to 50°C, this temperature range can be greatly extended using intelligent self-calibration algorithms. As temperature increases, several fundamental effects occur in circuits. As a rule of thumb NMOS and PMOS transistors have a threshold voltage shift V_T magnitude of roughly |2mV/K|; the NMOS coefficient has a negative sign and the PMOS coefficient has a positive sign. These threshold voltage shifts can be very detrimental to circuit operation. Also the bias voltage references and current sources can force transistors into the wrong region of operation and drastically reduce gain. In addition, the carrier electron mobility inside the transistor is a function of temperature (to the -1.5 power).

$$\mu(T) \propto \left(\frac{T}{T_{\text{Nominal}}}\right)^{-1.5} \tag{1}$$

Thus, circuits that are operating at high temperatures can experience severe carrier mobility degradation and drastically reduced NMOS drain-to-source currents. This results in reduced transconductance, and significantly shifts input and output impedances. Carefully constructed RF matching circuits work poorly when the transistor input and output impedances shift due to high temperature.

By knowing the specification values of interest via S-BIST, the self-calibration system can direct the circuit to perform better. As a part of the self calibration scheme, bias currents/voltages can be trimmed via DAC control to compensate for low mobility and transconductance, and varactors (variable capacitors) can be employed to control impedances. In this paper, we demonstrate the use of a DSP controlled programmable current mirror scheme, which determines the main bias current of the device. Figure 2 shows this bias circuitry where digital switches S_0-S_4 control the total current through the NMOS transistor.

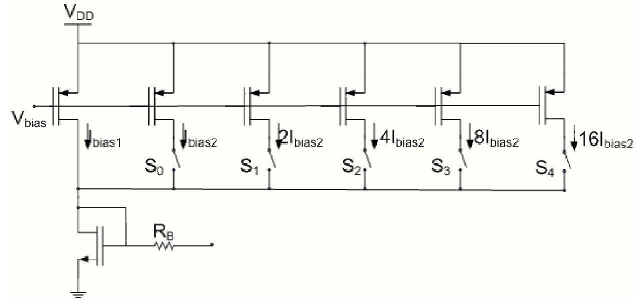


Figure 2. Programmable bias circuit.

The overall S-BIST driven self calibration scheme is shown in Figure 3. The self calibration procedure works as follows: (a) in the field or after manufacture, the self calibration mode is turned on depending on the application (self-calibration for thermal or process variation, respectively); (b) the DSP processor activates test stimulus generation process and switches device inputs accordingly; (c) the test response feature extractors are used to convert the test response into a DC/low frequency test response "signature"; (d) based on the pre-defined regression models described earlier, these signatures are mapped into the test specification values of interest in the presence of temperature and/or process deviations; (e) finally the DSP processor adjusts the digital control bits to trim the circuit bias point. The trimming process is iterated until the optimum operating point is obtained based on a predefined *optimization rule*.

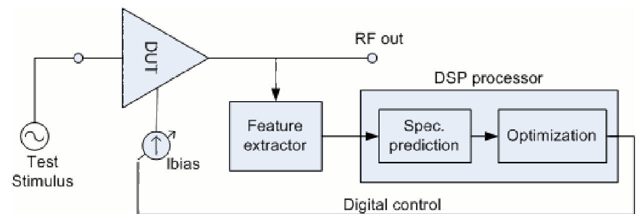


Figure 3. Basic scheme of S-BIST calibration.

In order to achieve good compensation, the optimization process needs to be driven by a goal function based on the optimum circuit performance. Depending on the circuit application and the distance between the nominal specification value and its bound, various methods are possible. For example, suppose that the noise figure requirement of a circuit is stringent, whereas the other specifications have enough performance margins. In this case, the calibration process focuses manily on noise figure performance. For diverse applications, the cost function $\Phi(x)$ for variable x (each variable is a bias

voltage or current that can be adjusted to compensate the RF circuit for performance loss) is defined as

$$\Phi(x) = \sum_i w_i \cdot f_i(x)$$

where

$$f_i(x) = \begin{cases} |S_i(x) - S_{i_T}|, \text{ if } S_i(x) \text{ is worse than } S_T \\ 0, \text{otherwise} \end{cases} \quad (2)$$

where w_i is a weighting factor, and S_i and S_{iT} represent the *i-th* specification value and its target specification bound, respectively. In this scheme, the minimum value of the cost function corresponds to optimum self-calibration. In general, some specifications may need to be compromised since their rates of change conflict with other specifications. For this purpose, the function $f_i(x)$ defines a margin around the target specification bound, where it is simply set to zero for specification values better than this boundary, otherwise to a positive value proportional to the distance from the boundary.

5. Simulation Results: Case Study

The efficiency of the proposed self calibration scheme is evaluated using a 2.4GHz CMOS LNA shown in Figure 4, designed using National Semiconductor's 0.18μm CMOS9 process technology. The specifications of interest are S_{11}, S_{21}, S_{22}, noise figure (NF), and 1dB compression point (C_{1dB}). As mentioned before, the proposed scheme is designed to extract the specification values of interest using alternate built-in test, which keeps the error of specification prediction below 0.2%. Based on the alternate test prediction accuracy discussed in the literature [10][11][12], we assumed that the specification value is extracted under ideal conditions.

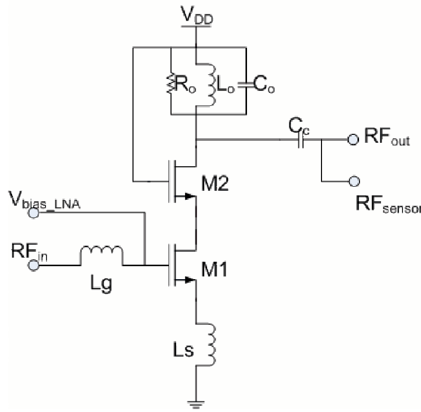


Figure 4. 2.4 GHz CMOS low-noise amplifier.

To adjust the bias current of the LNA, the programmable bias circuit shown in Figure 2 is used with 5 switches. The total current in the bias circuit is set to a range of 240μA to 880μA with a I_{bias1} value of 240μA and I_{bias2} value of 20μA. By scaling the ratio of M1 in Figure 4 to the NMOS transistor in the bias circuitry, the bias current of the LNA is approximately 10 times that of the total current from the bias network with a resolution of 200μA.

The cost function for optimization is defined for the target specification vector S_T : [S_{11} S_{21} S_{22} NF C_{1dB}] with the value of [-20 12.28 -20 2.125 -13.8]. Many instances of the circuit were simulated via Monte-Carlo simulation using predefined process variable statistics and the results of these Cadence-Spectre simulations were used for obtaining a min-max value pair for each specification. The weighting factors w_i are defined as the reciprocal of the differences between these min-max values, hence each product in $\Phi(x)$ was normalized to the specification limits for each specification.

5.1. Temperature calibration

In order to emulate large swings of temperature, the LNA circuitry with the nominal process variable values was simulated over the temperature range of -30°C to 70°C in steps of 20°C using the Cadence Spectre simulator. The capabilities of the proposed self-calibration scheme are demonstrated for the resulting 6 temperature points.

Table 1. Best & worst corners of each specification before and after temperature calibration.

Spec. [dB]	S_T	Original spec range: A	Spec range after calibration: B
S_{11}	<-20	(-26.6, -20.4)	(-31.2, -20.4)
S_{21}	>12.1	(11.2, 13.3)	(12.2, 13.2)
S_{22}	<-20	(-28.8, -23.9)	(-29.1, -21.4)
NF	<2.125	(1.45, 2.77)	(1.45, 2.45)
C_{1dB}	>-13.8	(-14.6, -13.3)	(-14.6, -13.7)

Table 1 summarizes the results of temperature effect calibration. The third and fourth columns in Table 1 show best and worst specification values among the 6 cases before and after calibration. For example, the best case specification S_{11} is -26.6 dB and the worst case value of the same is -20.4 dB. After calibration, the best value is improved to -31.2dB even though the worst value remains the same as before. Both of them meet the target specification bound S_T of -20dB. As can be seen from Table 1, the specifications S_{21} and NF are compensated to meet the specification bound S_T or approach the target specification bound S_T, with little degradation of the specification C_{1dB}. Both of the specifications S_{11} and S_{22} remain within the required bounds after calibration. In this example, even though all the specifications can not be

compensated effectively, some critical ones such as gain are compensated to remain in the region defined by S_T with a little or no degradation of the other specification values.

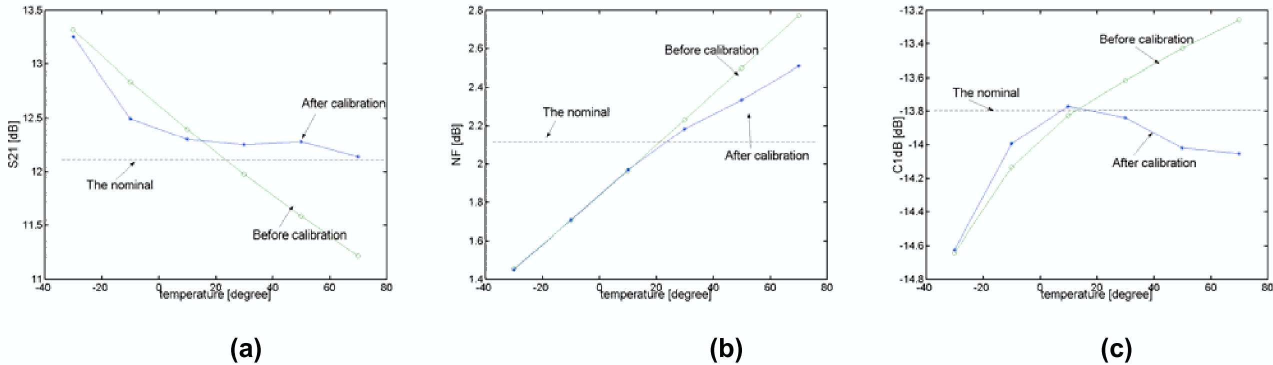
The plots in Figure 5 show the specification value changes after calibration for each temperature where the dotted line is an indicator of the nominal value. The optimum result is ideally assumed to be the flat specification value for various temperatures after calibration. Figure 5 shows that the specification S_{21} is well confined in the region defined by S_T while NF improves significantly due to compensation.

5.2. Process variation calibration

In the presence of process variations, the self-calibration ability of the proposed methodology is demonstrated on a number of LNA instances each representing statistical corners for different specifications. These statistical corners present the worst and best instances for each specification performance, which are obtained through Monte Carlo simulations.

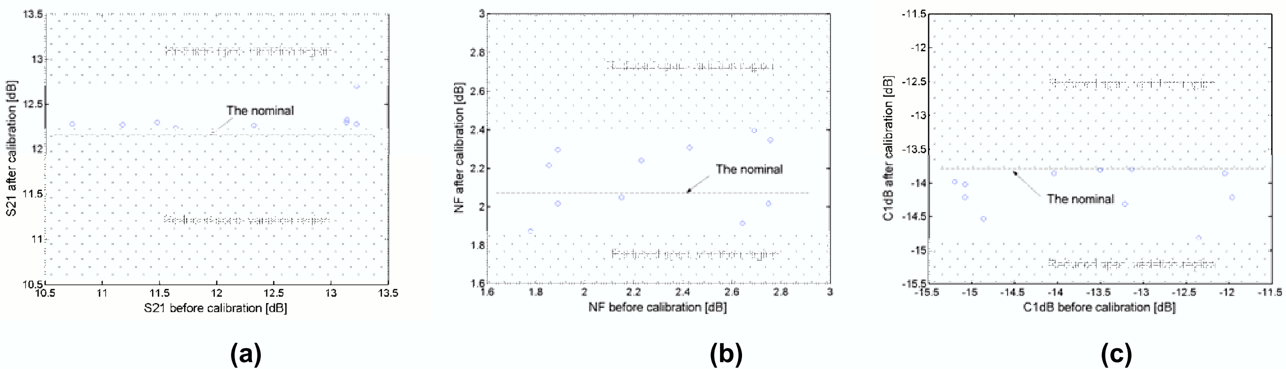
The optimization metric is driven by an objective function that is based on minimizing the deviation in each specification in the presence of process variations. It is important to note that this objective function is just an example and may not be the best for every specification. For example, minimal variation around the nominal value is most desired for S_{11}, S_{22} and generally for S_{21}, whereas NF/C_{1dB} are better when minimized/maximized. In this sense, we assume that the figure of merit for evaluation is the change in specification variability after calibration, which can be measured by the ratio of the specification variation range after calibration over the one before calibration. For successful calibration, this ratio should be smaller than 1, and smaller values represent better compensation. In this sense, the statistical corners are perfect candidates for the evaluation set, since they have the largest deviation from the nominal and hence provide the biggest challenge for the proposed self-calibration scheme.

The specification ranges before and after calibration are shown in Table 2 where the second column shows the minimum and maximum specification values for each specification before calibration and the third column shows the specification ranges after calibration. The last column displays the figure of merit, *R*, which is the ratio of the specification range after calibration over the one before calibration. For example, the specification S_{21} shows 13.2dB and 10.5dB as the minimum and maximum values for the circuits before calibration. After calibration,



(a) (b) (c)

Figure 5. Calibration of temperature effect for; (a) S_{21}, (b) NF, and (c) C_{1dB}.



(a) (b) (c)

Figure 6. Calibration of process variation effect for; (a) S_{21}, (b) NF, and (c) C_{1dB}.

theses extreme values shrink to 12.2 dB and 12.7dB, thus achieve the ratio of 0.1722. Table 2 shows that *R* is smaller than 1 for each specification of interest, hence the proposed calibration technique is successful.

The scatter plots in Figure 6 show the calibration of the specifications S_{21}, NF, C_{1dB} where the x-axis corresponds to the specification value before calibration and the y-axis the same value after calibration. As these examples suggest, the wide range of variation is dramatically reduced for all specifications after calibration.

In the above experiment, the evaluation set utilizes the worst instances, which are, in general, out of the test pass/fail thresholds, resulting in a fail during production test. However, using the calibration process these instances can be operated in the pass-region. As a result, the circuit with an S-BIST scheme can increase production yield due to this added value, despite the additional circuitry and area-overhead.

Table 2. Best & worst corners of specification values before and after calibration for process variations.

Spec. [dB]	Original spec range: A	Spec range after calibration: B	Ratio: R (B/A)
S_{11}	(-42.5, -16.5)	(-31.3, -17.5)	0.5288
S_{21}	(10.5, 13.2)	(12.2, 12.7)	0.1722
S_{22}	(-27.5, -15.5)	(-25.9, -15.6)	0.8574
NF	(1.78, 2.75)	(1.87, 2.39)	0.5349
C_{1dB}	(-15.19, -11.96)	(-14.8, -13.8)	0.3168

6. Conclusions

In this paper, a self-calibration technique (S-BIST) is described to address large performance variability due to temperature and process variations. RF built-in alternate test techniques are utilized to extract the specification values in the presence of temperature and process deviations. After this diagnosis, self-calibration is performed by adjusting circuit bias parameters. The proposed scheme is demonstrated on a 2.4GHz LNA, by adjusting the bias current to maximally compensate for performance deviations. Based on the simulation results, the proposed self calibration scheme can significantly reduce process variation effects, resulting in enhanced circuit yield and better reliability in the presence of temperature deviations. In on-going research, the proposed self-calibration technique is being applied to RF receiver systems.

7. Acknowledgements

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