Temperature Compensated Built-In Alternate Test of RF Modules

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Abstract

At low frequencies, alternate testing of analog modules is based on sampling the test response using an A/D converter and analyzing the digitized response in the external tester. In order to use alternate test at frequencies in the multi-GHz range with RF components, both the test waveforms need to be very simple and the evaluation of the test response should be handled by practical hardware-based test response feature-extractors. One such scheme employs sensors that measure a complex function of the response waveform and output a DC signature which can easily be collected by a low-cost external tester or can be evaluated by system resources available on chip/package. In this work, we demonstrate the first temperature compensated alternate test, which makes use of built-in feature extraction sensors. The simulation study on a 900 MHz low-noise amplifier (LNA) shows accurate prediction of IIP3, 1dB compression point and noise figure specifications even when the operation temperature of the LNA is not monitored by external means throughout the testing process.

1. Introduction

Despite the differences in many methodologies to implement manufacturing test of analog circuits, the challenge of keeping up with the ever-increasing operating frequency of the device-under-test (DUT) remains a key factor. Although progressive studies in advancement of automatic test equipment (ATE) suggest that ingenious design and black magic in innovation can yield ATE systems that perform right on the edge to satisfy specification coverage, the cost of such high-end systems induce a prohibitive block to initial cost as well as comprehend a handsome percentage in the manufacturing cost of each good-known-package due to long test times accumulated as a result of many separate tests each covering one specification in the datasheet. Furthermore, with each new generation of analog system technology, increasing integration closes the open fields that ATE engineers can explore to account for the gap between the systems they test and the systems they design to test others. These challenges initiate a paradigm shift in high-speed analog testing favoring alternative approaches such as built-off test (BOT) and built-in test (BIT) where the test functionality is brought to the closest possible proximity of the DUT, that is to the load board for BOT and into the chip/package for BIT. Both schemes can make use of a low-cost external tester connected through a low-bandwidth link in order to carry on the demanding evaluations, as well as make use of the analog-to-digital converters (ADC) and digital signal processors (DSP) on the chip/package to extend the methodology with a self-test flavor (BOST and BIST). In applications like systems-on-packages (SOPs) the test problems such as signal integrity, I/O bandwidth, and limited controllability and observability dictate BIT a necessity rather than an alternative enabler technology. Although recent research on analog BIST proposed hardware solutions for single specifications, the paradigm shift calls for a rather general approach where a single methodology can be applied across different devices and multiple specifications can be verified through a single hardware minimizing area overhead. Furthermore, any such approach has to come equipped with features to address the environmental and process variation effects on the test circuitry itself, since anything contributing to the parametric faults under investigation may as well despair the way BIST performs.

In this paper, we propose an extension of the alternate test methodology that is suitable for BIT of multi-GHz analog and radio-frequency (RF) components packed in an integrated environment. The fundamentals are handled in Section 2, where we review the alternate test methodology, discuss its challenges in multi-GHz test and summarize the solutions proposed. Section 3 elaborates on one such solution, namely DC level feature extractors; we discuss the disadvantages of classical sensors such as peak or rms detectors and introduce a new class of sensors that can better explore the possibilities proposed by alternate test methodology. Section 4 gives the details for an implementation of these implicit feature extraction sensors as well as an extension of the algorithm for a temperature compensated BIT. In this implementation, we demonstrate that our proposed methodology is general enough to address environmental effects on the BIT circuitry. The results of this experiment are summarized in Section 5.

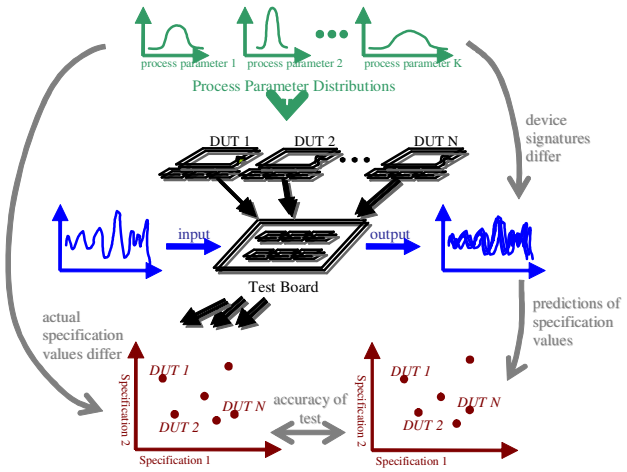

Figure 1: Alternate test methodology.

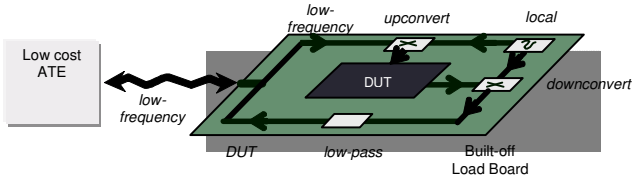

Figure 2: Modulator/demodulator based built off test scheme.

2. Alternate Test at Multi-GHz

The classical production testing approach to specification based analysis makes use of a large set of functional tests that add significantly to the test time and final cost of the integrated circuit. On the other hand, fault based testing provides an inexpensive alternative to functional tests, but it usually fails to consider the parametric fault effects and the results may not have a direct significance in terms of data sheet specifications. *Specification-based alternate tests* propose a way to bridge the gap between these two methodologies. In this scheme, the data sheet specifications of a DUT are predicted by analyzing its response to a specific input pattern, which is carefully crafted to yield a significant correlation between the response and the specification variations. The DUT response can be considered as a signature for the effects of process variations specific to that DUT instance. These process variations also make the specification values derive from their ideal values. Figure 1 depicts this relationship.

The main theory behind specification-based alternate test is given in [1]. The variations in any process variable in the circuit parameter space P, affect both the circuit specification space S, and the response measurement space M. Two different non-linear mappings define these relationships: $f_{ms}: P \rightarrow S$ and $f_{pm}: P \rightarrow M$. Hence, for a region of acceptance in the specification space, there exist corresponding acceptance regions in the parameter space as well as in the measurement space. An instance of the DUT can be declared faulty if its corresponding measurement data resides outside the acceptance region in M. Furthermore, nonlinear statistical multivariate regression analysis allows one to construct another function $f_{ms}: M \rightarrow S$ such that for a given set of measurements, the mapping generates predictions for the values of specifications-under-test.

This way alternate test goes beyond discrete pass/fail decisions and can be used for performance evaluation of an instance of the DUT.

Section 4 in [2] covers an extensive bibliography of recent research on analog BIT and BOT [3-14]. These implementations propose customized hardware solutions good for single specifications-under-test, which introduces significant area overhead since multiple specification measurements require different kind of resources. Furthermore, most of them only provide pass/fail decisions in the presence of catastrophic faults. There are only a few new approaches, such as [15], which can generate quantitative measures for selected number of specifications; however, the measurement-to-specification mappings have to be hand crafted specifically to the characteristics of the DUT. On the other hand, specification-based alternate test provides a general methodology independent of the DUT or the target specifications. In this sense, it is a complete tool which can be applied across different devices, and multiple specifications can be verified through a single hardware minimizing area overhead.

At low frequencies, alternate testing of analog modules is based on sampling the test response using an ADC and analyzing the digitized response in the external tester. The sampling of the signature is a critical part of the alternate test such that the speed and accuracy of sampling mostly defines the accuracy of predictions. For RF components operating in the gigahertz range, this requirement defines a problem, since the Nyquist sample rate of such signals and their harmonics may far exceed the capabilities of ADCs already present on-system. Even if such ADCs are present on-system, they introduce significant area overhead and signal degradation when interconnected as a part of the BIST scheme. In order to use alternate test at frequencies in the multi-GHz range with analog and RF components, both the test waveforms need to be very simple and the evaluation of the test response should be handled by some way avoiding high speed A/D conversion. First such methodology is proposed in [16], where a rich baseband signature is modulated to GHz range by a carrier and the response is demodulated back to baseband. Although this scheme -given in Figure 2- avoids high speed A/D, it

requires high speed upconversion and downconversion circuitry driven by carriers carefully separated by a few MHz. Such an implementation imposes a large area overhead and hence is feasible for BOT only. As a result of this, in [17], we have developed an optimization scheme to solve for the simplest possible input stimulus that can satisfy predefined prediction accuracy. When simplicity is defined in terms of frequency, this scheme comes up with a sinusoidal input stimulus, frequency of which is two orders of magnitude smaller than the original operational frequency of the DUT. Although this solution relaxes the constraints on stimulus generation circuitry and response digitization, it can only partially cover matching problems and frequency-dependent radiation effects caused by closely spaced conductors. Another GHz-range alternate test methodology [18] implements a digital-BIST [19] friendly approach. It makes use of a high frequency sinusoidal as the input stimulus and digitizes the response by a single-bit comparator. It is basically a subsampler extracting reliable spectral features of the response, which can take care of coherence and phase noise problems as well as tolerate imperfect input stimulus. When compared to the previous two alternatives, its disadvantage comes in terms of a longer testing time, since the response feature extraction works in a statistical fashion.

Apart from these three implementations of high-speed alternate test – upconversion / downconversion, testing with lower frequency stimulus, spectral feature extraction by reliable subsampling -, there is a fourth class of methodologies that recently presented promising results. In this approach, hardware based test response feature-extractors are utilized to produce a DC level signature of the alternate response obtained from DUT. In [20], common peak detectors are used to serve as feature extractors, and peak values of the signal at various stages are used together to predict end-to-end specifications of the system as well as individual specifications of some of the modules. Although this experiment demonstrates the potential of DC level sensors used together with alternate tests, the explicit features, such as peak or rms, do not make full use of the power in alternate mapping process. Instead, one can replace these common sense detectors with implicit feature extractors. When designed with alternate test in mind, such implicit detectors extract DC features that exhibit hardly any correlation for the bare eye, but in fact can be impressively rich in terms of correlation for the alternate mapping process.

In this paper, we propose a methodology to extend specification-based alternate tests in a way to accomplish low-cost built-in self-test of RF components using implicit feature extractors. The next section compares the use of implicit versus explicit feature extractors in the light of exploring possibilities proposed by using alternate test methodology.

3. DC Level Feature Extractors

DC level feature extraction is not a new concept; the idea has been used in measurement setups in order to study the properties of a waveform, which is otherwise not completely characterized. The most well known examples of such extraction circuitry are in the form of peak or root-mean-square detectors. Other common examples are zero-crossing detectors, bias current/voltage sensors and tuned spectral component detectors. These extractors are common because the DC values they represent can be easily related to a physical property of the original AC waveform, hence explicit. Such DC properties and their corresponding sensor structures, *explicit feature extractors*, can be directly used with alternate test [20] to produce predictions for specifications-under-test.

However, there are many challenges in the implementation of explicit feature extractors. The DC values they present are almost always approximations to the original feature –peak, rms, etc- under a long list of assumptions such as waveform type, frequency and swing ranges or piecewise fitting. The deviations are usually a result of the non-linearity present in the semiconductors making up the detector. In this sense, highly linear devices such as bipolar transistors are preferred over field effect transistors, which generates a bottleneck given that the range of bipolar devices available in modern processes are very limited. Even bipolar based applications require a calibration scheme in post-production, when the accuracy is a key element. This calibration step is reflected to the manufacturing cost of the device in terms of extra time and real estate overhead. Furthermore, when these sensors are built-in, they are affected by the same process variations and environmental effects that degrade the performance of the DUT. In order to make them immune to these variations, the designer can add additional circuitry; however this approach makes the sensor larger and more complicated. If the DUT is a RF component, where simplicity is a key element, the sensor may become even larger than the device, shifting the focus to the sensor rather than the DUT since the former will be more susceptible to faults.

As an example, let's consider the peak detector proposed in [21]. In this paper, the peak detector is made up of two bipolar transistors, one connected single-ended to the input. The transistors are arranged to produce a differential output, one side of which is used to cancel the DC bias. This implementation is selected as an example because its differential nature helps protect against process and environmental variables; furthermore, it provides a linear mapping when compared to field-effect transistor-based or diode-based peak detectors, yet keeping a simple structure with low transistor count. Following all these properties, it represents a high-end example for

common explicit feature extractors. However, even this implementation needs calibration for specific regions of operation. Moreover, its output is proportional to the peak of the signal provided that the signal is a sinusoidal. For distorted waveforms its accuracy fades dramatically destroying the one-to-one mapping. In [22], Zhang et al show that its relative error in representing the peak value goes up to 900% for a transition region in its transfer characteristics. So, any application making use of this detector should implement a calibration procedure for this region. In [22], a hardware modification is proposed to implement a more linear transfer function, keeping its relative error in the 8%. On the other hand, this modification makes the implementation more complicated, and adds significant area overhead. Our experiments suggest that in the presence of regular process and temperature variations, the relative error for the original circuit is 42% excluding the problematic transition region, and the error goes up to 63% after hardware modifications proposed in [22]. Hence, the performance of this detector in a built-in test environment is unsatisfactory for the common process and environmental variations affecting the original DUT.

The problems depicted for the example above are characteristic for explicit feature extractors. In this case, the circuitry functions as a peak detector only under a long list of assumptions, which can easily be violated in a built-in test environment even when some form of calibration is provided. As a matter of fact, the DC signature for this sensor presents a richer content than a single peak value. In favor of being able to build the correlation relation easily, the user constrains its potential ability by settling down to an approximation of a one-to-one mapping by ignoring its nonlinearity and variation under non-ideal sinusoidal inputs. In contrast, if the output of such a sensor is used with alternate test methodology, the inherent mapping process will make better use of its richer signature content instead of treating it as a distorted approximation of a peak value. In other words, the implicit features of the signature are made explicit by the mapping process. Moreover, the process provides inherent calibration for problematic operating regions as well as process and environmental variations. By using alternate tests with very simple sensor structures, one can have high-end results which are otherwise only possible with elaborate post-production calibration and additional complex circuitry to take care of variation effects. This presents a new sensor paradigm for use with alternate test methodology. Since the measurements in alternate tests are different from those made in classical specification based tests, the built-in sensors used for measuring classical figures of merits such as peaks, root-mean-square values, zero-crossings, etc can be replaced with *implicit feature extractor hardware* that measure figures that are more accessible but harder to relate to the specification value. Although this relation is not easy to build, the mapping process in alternate test will build a good enough prediction as long as the changes in the measured figure are correlated to the specifications under test. In order to validate the idea, we take the simple peak detector in [21], and study its signature characteristics when its input is not bounded by assumptions. After studying these implicit features, we will be able to modify the sensor to generate a class of sensors, which can be used together to predict complex device specifications such as the third order intercept point (IIP3), 1 dB compression point (1dBCmp) and noise figure (NF) instead of a single peak value. Furthermore, we show that alternate test provides an inherent calibration when the sensors as well as the DUT are subject to large temperature variations.

4. Implementation of Feature Extractors

Figure 3 shows the peak detector in [21]. Let's dissect the input waveform into a bias voltage and $x(t)$ such that: $V_i = V_B + x(t)$, and define $V_C = V_B - V_A$; $V_C' = V_B - V_A'$. Then for Q_1 and Q_2 being identical:

$$I_{C1} = I_{S1} e^{\frac{V_C}{V_t}} e^{\frac{x(t)}{V_t}}$$

$$I_1 = I_{S2} e^{\frac{V_C'}{V_t}}$$

$$I_{C1}\Big|_{dc} = I_{S1} e^{\frac{V_C}{V_t}} \left| e^{\frac{x(t)}{V_t}} \right|_{dc} = I_1$$

$$e^{\frac{V_C}{V_t}} \left| e^{\frac{x(t)}{V_t}} \right|_{dc} = e^{\frac{V_C'}{V_t}}$$

$$e^{\frac{V_C' - V_C}{V_t}} = e^{\frac{x(t)}{V_t}} \Big|_{dc}$$

Since $V_o = V_A - V_A' = V_C' - V_C$;

$$V_o = V_t \cdot \ln(e^{\frac{x(t)}{V_t}} \Big|_{dc}) \qquad \text{equation } \alpha$$

The derivations in [21] and [22] depend on the assumption that when $x(t)$ can be represented with a sinusoidal, a modified Bessel function can be used to compute an approximation of the DC value for $exp(x(t)/V_t)$. Equation α is a generalized version of this derivation without any extra assumptions.

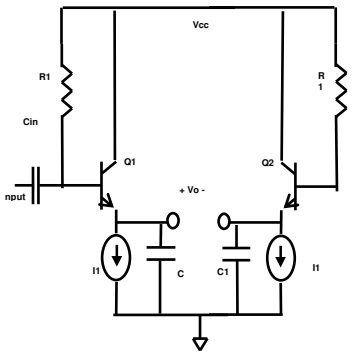

Figure 3: Exponential mean

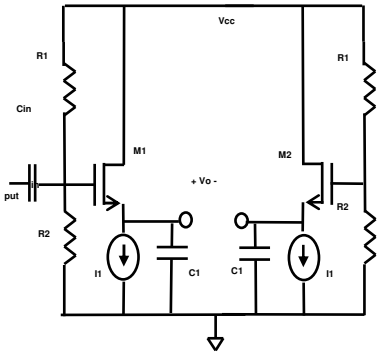

Figure 4: Square mean

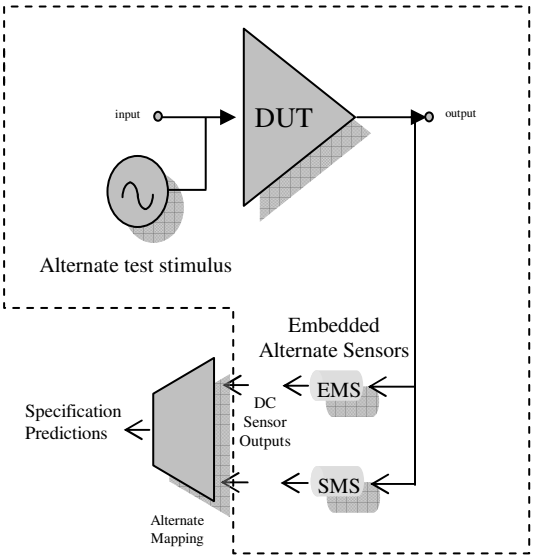

Figure 5: BIT setup with orthogonal

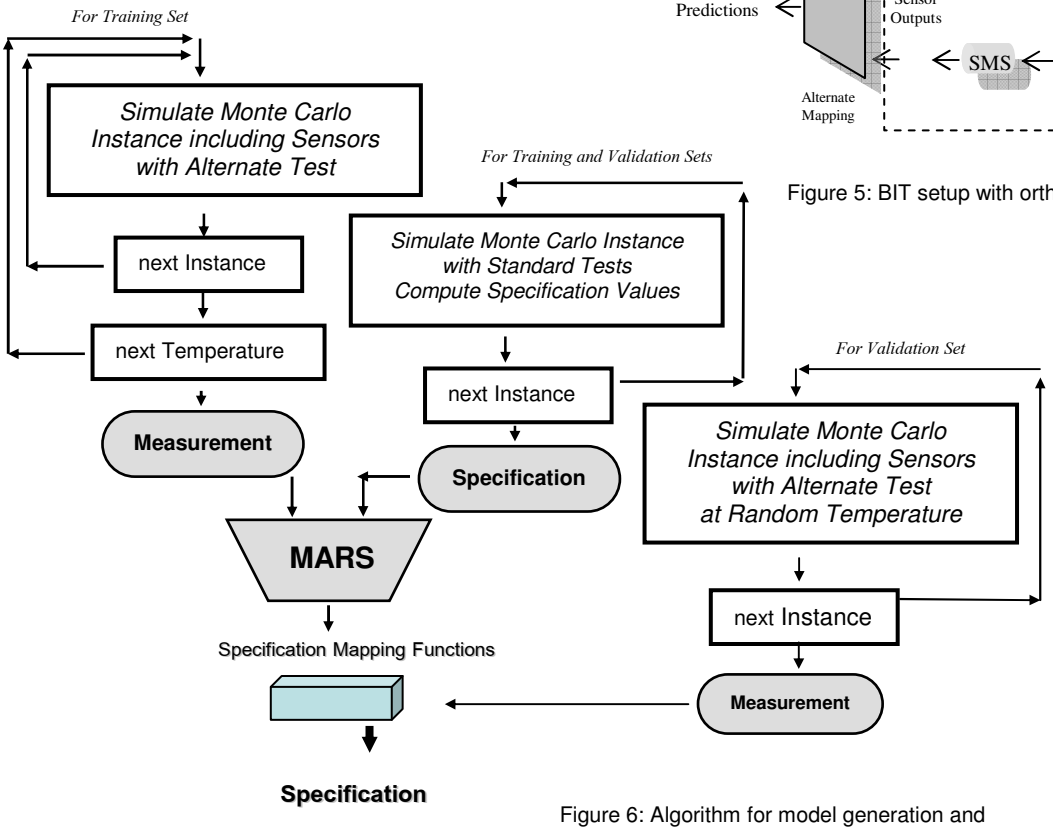

Figure 6: Algorithm for model generation and application.

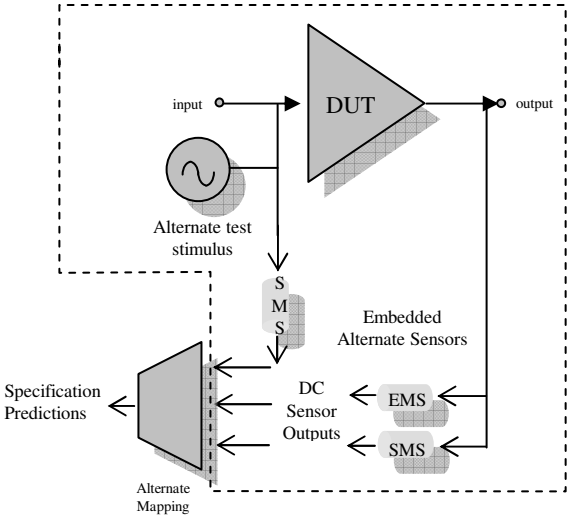

Figure 7: BIT setup with orthogonal sensors and a third sensor

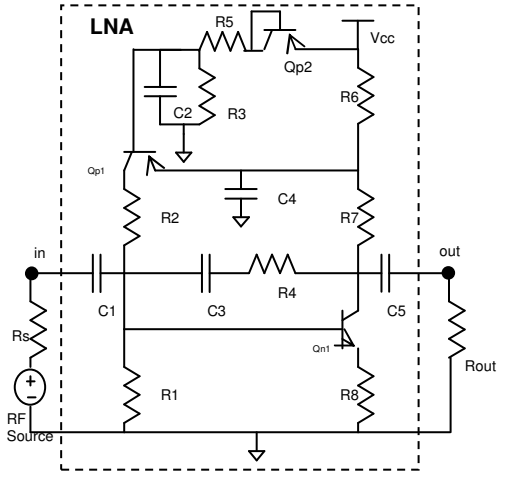

Figure 8: Schematic of the 900 MHz low-noise

Although the detector in Figure 3 can be used with alternate tests to predict the peak value of the sensor input, prediction of more complex specifications such as IIP3 or NF demand extra dimensions for the measurement space. Therefore, alternate test mapping functions need at least one other detector. Instead of carefully searching for one, we propose a generic way to generate a class of sensors from a single architecture. Equation α is the form of $V_{o1} = f_1(mean(e^{g_1(input)}))$, where exponential characteristics come from the bipolar transistor. Figure 4 shows the second detector, when the bipolar devices in Figure 3 are replaced with field-effect transistors. These two sensors are also "orthogonal" in the sense that both make use of the same topology but with different active components, which change the function that is mapping the peak values to the measurements. In this case, the logarithmic/exponential relation given in equation α is replaced with a square root/square relation yielding equation β in the form $V_{o2} = f_2(mean(g_2(input)^2))$. Figure 5 shows the BIT setup using these sensors, namely *exponential mean sensor (EMS)* with the BJTs and *square mean sensor (SMS)* with the FETs. A simple on-chip/package analog signal generator applies the test stimulus to the DUT through a test multiplexer. The *orthogonal sensors* output two DC values to be sampled by the low-cost external tester. These DC values are fed into the specification mapping module in the external tester and non-linear mapping functions output predictions for specifications-under-test.

The non-linear mapping function from measurement space to the specification space is constructed by the methodology named multivariate adaptive regression splines (MARS) [23]. The model can be visualized as a weighted sum of basis functions made of splines, which span all values of each of the independent variables. The MARS model for a predicted specification y with M measurements can be summarized as:

$$y = f(x) = \beta_0 + \sum_{m=1}^{M} \beta_m H_{km}(x_{v(k,m)})$$

where, the summation is over the M independent variables, β_0 and β_m are parameters of the model, and the knots t defines the basis functions. H is defined as

$$H_{km}(x_{v(k,m)}) = \prod_{k=1}^{K} h_{km}$$

where $x_{v(k,m)}$ is the k^{th} independent variable of the m^{th} product. During the forward stepwise placement, basis functions are added to the model. After this step, a backward procedure is applied and the basis functions associated with the smallest increase in the least squares fit are removed, producing the final model.

Two sets of device instances are generated for training and validation purposes using the circuit netlist, device models, and process variable distributions. SpectreRF™ simulator is used to simulate all of these instances at the nominal operating frequency and at the nominal temperature of operation. These simulations are designed to measure actual specifications of interest for each circuit instance. Then, these models are used with the validation set to generate predictions of specifications-under-test. In order to validate the auto-calibration ability, the test algorithm is modified to train the MARS mapping at different operating temperatures. Figure 6 shows the details of this algorithm. The same set of training instances are simulated at different district temperatures and mapping is built to predict the original specifications at the nominal operating temperature, which corresponds to the datasheet specifications. The verification set is generated over random temperatures in the training temperature range; hence there is no direct link from the temperature the sensor readings are made to the MARS models. In this experiment a third sensor, which is an exact copy of one of the orthogonal sensors, is directly connected to the input of the DUT, and the DC output is fed into the mapping module with the other two sensor outputs. Figure 7 shows this configuration in which the additional sensor acts as a temperature monitor.

5. Experiment Results

In this section, we demonstrate and validate the proposed architecture by a series of simulation experiments. Our test vehicle is a 900 MHz low-noise amplifier (LNA). Figure 8 shows the schematic of the LNA with 8 resistors, 5 capacitors, and 2 transistors; this particular LNA is chosen as the test case because it is available to public in Cadence RF libraries [24]. The saturation current and the forward gain of the transistors, together with sheet resistance make up 5 process variables. Each process variable is assumed to have a normal distribution with $3\sigma = nom/10$, where *nom* represents the nominal value for the variable, and σ is the standard deviation. The validation set is a 100 sample random set with the specified jointly normal distribution. The training set is composed of two parts, the first one is a 50 sample jointly normal distribution; whereas the second part is another 50 sample random set with process variables linearly distributed over the ±10% range around the nominal values. The validation and training set instances are generated by the Monte Carlo method. The specifications of interest for the LNA example are chosen such that each one emphasizes a different aspect of transient testing. The sample specifications are 1dBCmp, IIP3, and the NF at the nominal operating frequency. The 1dBCmp is a good figure of performance for single tone

inputs, whereas IIP3 is typically measured by two-tone inputs. Noise figure presents a specification that is highly frequency dependent. The corresponding alternate test stimulus is a 900 MHz sinusoid. A single sinusoid is selected in favor of its simplicity to be generated on-chip/package by a local oscillator or be supplied from a low-end external source.

The experiment is designed to be performed in 6 steps, each investigating a controlled branch in the space of possible experiments. The 1st step checks prediction errors for the LNA, when the DUT analog response samples are used directly to generate the regression models and to predict the specification values of the validation set instead of orthogonal sensor outputs. Although sampling at that frequency is not feasible for a BIT application, these results represent an ideal limit for alternate test predictions without the DC level feature extractors and listed for comparison. Similarly, the 2nd step uses analog response samples only this time for the validation of the auto-calibration ability. For every auto-calibration experiment, the 100-instance training set is simulated at 6 discrete temperature values -20, 0, 20, 27, 40 and 60˚C; then, a new 400-instance validation set is generated by 4 copies of the original 100-instance validation set. Each instance in this new validation set is simulated at a random temperature in the range [-20, 60] ˚C. The 3rd step of the experiment implements the structure in Figure 5, while 4th step runs an auto-calibration experiment with the same setup in the absence of the third sensor acting as a temperature monitor. The 5th setup challenges the ability of the square-mean sensor as an explicit temperature monitor; in this experiment, the simulation temperature is provided to the training set explicitly and MARS mappings are generated for temperature using only the third sensor. Figure 9 shows the setup for this experiment. Finally, the 6th step of the experiment validates the proposed auto-calibration methodology depicted in Figure 7.

Table 1 shows the summary of results for all six steps. For each case, the maximum prediction error is listed as the absolute difference from the original specification. As a matter of fact, errors represented in percentages of the original value give a better idea about the accuracy of the prediction. However, some original IIP3 values are in the close proximity of 0 dB, hence even a very small error in prediction of these values gives a misleading impression yielding to very large percentage errors. When referring to percentage errors we will discard these values around 0dB. A better way to compare prediction accuracies is a constellation graph, a 2D visualization in which x and y coordinates of every point correspond to actual and predicted specification values respectively. An ideal prediction is represented by a 45˚ line, and the deviations from this line define prediction accuracy. If the overall goal of the test is evaluating a pass/fail decision rather than

TABLE I. MAXIMUM PREDICTION ERRORS OF THE ACTUAL SPECIFICATION VALUES

#	Temp		IIP3	1dbC	Noise Figure*
1	**No**	**Ideal samp.**	*0.072 dB*	*0.092 dB*	*0.0081*
2	**Yes**	**Ideal samp.**	*3.2 dB*	*4.8 dB*	*1.19*
3	**No**	**2 sensors**	*0.41 dB*	*0.52 dB*	*0.25*
4	**Yes**	**2 sensors**	*3.3 dB*	*4.7 dB*	*1.23*
5	**Yes****	**2+1 sensors**	*3.3 dB*	*4.7 dB*	*1.23*
6	**Yes**	**2+1 sensors**	*0.62 dB*	*0.94 dB*	*0.19*

* at 900 Mhz ** Temperature as an explicit property

quantitative determination of specification values, then the prediction accuracy is more important in the close proximity of the decision boundaries for that specification. In this case, a large prediction error for an actual specification away from the decision boundary may not change the pass/fail decision, while a very small error for one on the decision boundary will likely cause a misclassification. In order to account for this measure, we will also include number of misclassified instances while comparing results of different experiments. Therefore, the numbers in Table 1 should always be considered together with secondary measures such as percentage errors and number of misclassifications.

In order to validate the ability of orthogonal sensors to predict complex specifications, one can compare the results of setups #1 and #3. Both of these experiments are performed at a constant temperature. In the ideal sampled case of #1, the maximum percentage error is 1.1%; whereas in #3 using DC signatures of the orthogonal sensors, the error goes up to 6.2%. Although this error is significantly larger than the ideal one, the accuracy is still comparable to the error resulting from the repeatability of a classical test measurement. Furthermore, the misclassification rate is the same for both setups, 1 out of 100 instances. Figure 10 shows the constellation graph for setup #3.

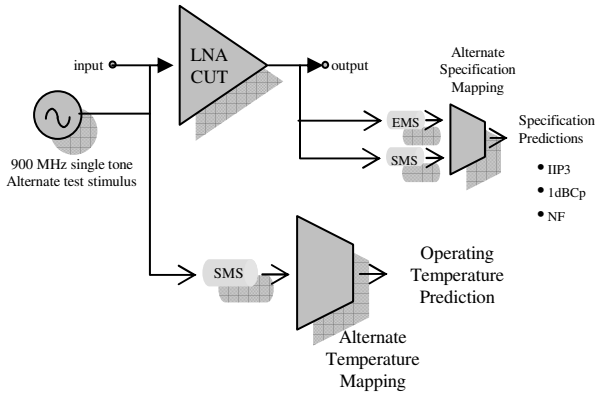

Figure 9: BIT setup for temperature prediction

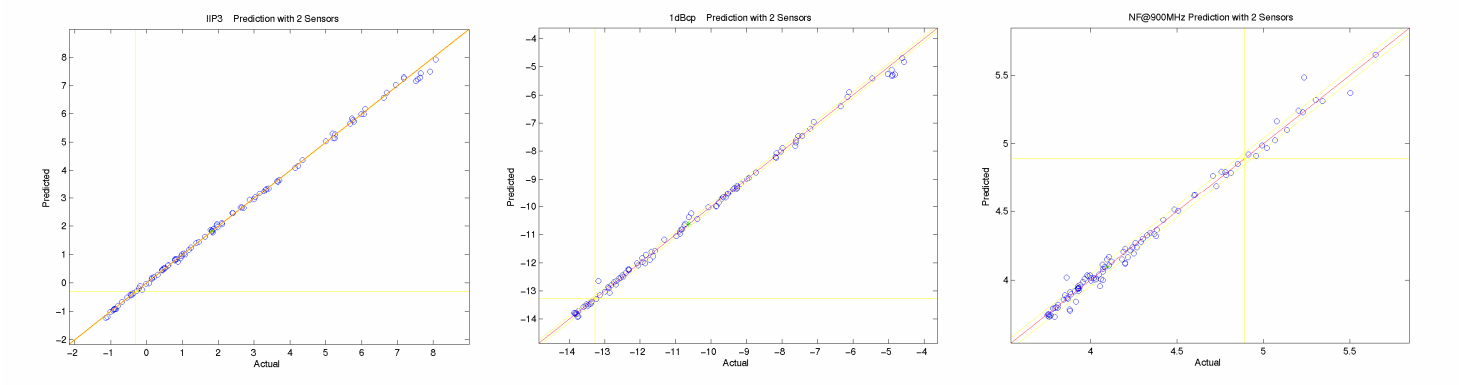

Figure 10: Predicted vs actual specifications for LNA with 2 orthogonal sensors.

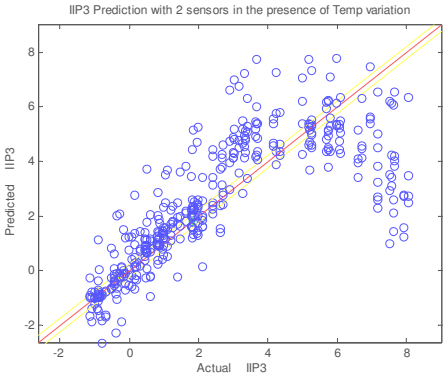

Figure 11: IIP3 Prediction without temperature monitor.

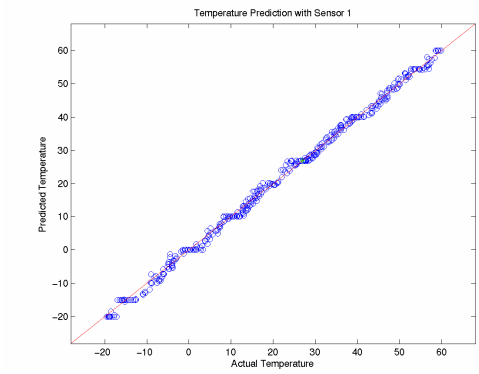

Figure 12: Temperature Prediction with temperature monitor.

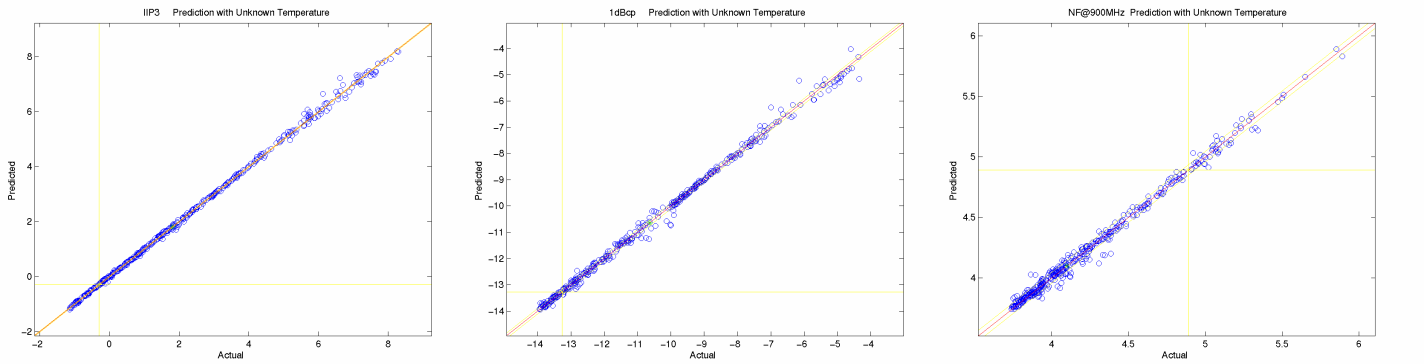

Figure 13: Predicted vs actual specifications for LNA with 2 orthogonal sensors and temperature monitor sensor.

When setups missing the temperature monitor sensor are compared with the corresponding setups performed at constant temperature - that is #2 versus #1 and #4 versus #3 -, the error percentages are observed to go up significantly, yielding similar misclassification rates around 21%. Although the predictions for the instances simulated at around the nominal temperature are similar in terms accuracy, the rest of them result in significant deviations from the 45˚ line. This hazy constellation graph is depicted in Figure 11 for IIP3 measurements in setup #4.

Setups #5 and #6 are performed in the presence of the third sensor as a temperature monitor. In #5, the signature of this additional sensor is only used for prediction of temperature as an explicit goal; hence, the specification predictions are not different from those in #4. The purpose of setup #5 is not to enhance the specification prediction, but to validate the use of the additional sensor as a temperature predictor. Figure 12 shows the results from the temperature mapping module, the maximum error is 3.37˚C and the rms error is 1.20˚C. Finally, setup #6

validates the proposed auto-calibration methodology. In this case, temperature is treated as an internal variable, and the DC signature of the third sensor is used with the other two to directly predict specifications-under-test. Figure 13 shows the constellation graphs for this setup, where the maximum percentage error is 8.1% and only 3 instances are misclassified out of 400.

6. Conclusion

The recent literature on specification-based alternate test has shown that by using alternate testing the test specifications can be predicted very accurately, significantly reducing the cost. In order to use alternate test at frequencies in multi-GHz range, both the test waveforms need to be very simple and the evaluation of the test response should be handled by practical hardware-based test response *feature-extractors*. These specialized analog circuits extract response signal waveform features in the form of low-bandwidth analog output signals. Furthermore, the built-in sensors used for measuring explicit figures of merits such as peaks, rms values, zero-crossings can be replaced with *implicit signal feature extractors,* which can make better use of the powerful mapping engine embedded in alternate test methodology. A case study suggests that this scheme can predict the IIP3, 1dB compression point and noise figure specifications of a 900 MHz low-noise amplifier with maximum errors of 0.41dB, 0.52dB and 0.25 respectively. Furthermore, mapping can serve as an auto-calibration capability for these sensors, which is validated in the case of temperature variations. The work is currently being extended to even simpler detector structures that can serve as process variation sensors.

Acknowledgment

This research was supported in part by the Packaging Research Center at Georgia Tech and by GSRC - MARCO 2003-DT-660.

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