

Optimal Multisine Tests for RF Amplifiers

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Abstract — With trends towards higher speed circuits, the cost of testing is beginning to dominate the overall manufacturing cost of high-speed components. To solve this problem, test complexity must be reduced dramatically. Prior research indicates that complex specification tests can be replaced by simpler tests from which many specification values can be extracted concurrently. In this paper, an optimal multisine test generation approach for RF amplifiers is presented. The goal of the paper is to examine tradeoffs between test complexity and process-variation induced failure coverage. It is shown that some complex specifications can be tested accurately using test signal frequencies significantly below the operating frequency of the RF circuit-under-test.

Index Terms — Multitone sinusoidal input waveform, radio-frequency circuit testing, automated test pattern generation, automated test pattern optimization.

I. INTRODUCTION

As wireless communication increasingly permeates everyday life, increasing production and integration of radio-frequency subsystems increases the demand for novel testing methodologies. Complex and very high speed test equipment is required for testing of radio-frequency component specifications. Furthermore, testing of specifications like the third order intercept point (IIP3) typically requires iterative sweeps of parameters. This increases the total testing time adding significant cost to the test budget. Complex radio-frequency system-on-a-chip implementations (such as of the Bluetooth™ standard) push the limits of testing techniques [1], and demand test pattern generation algorithms that are highly aggressive in terms of fault coverage and test time.

A competitive radio-frequency circuit testing methodology should (a) have high fault coverage even at speeds lower than the nominal operating frequency, (b) be capable of testing multiple specs concurrently, decreasing the total time necessary to validate all specs and (c) employ simple and easy to generate test input patterns in order to ease the need for complex automatic test equipment.

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II. MOTIVATION

In this paper, we present a test pattern generation algorithm that optimizes a single multitone sinusoidal input waveform in such a way as to detect all manufacturing defects and process variations that also affect the test specifications of the device under test (DUT). The cost function is defined in terms of several design variables such as the maximum input frequency, testing time, test coverage, etc. The multitone transient input is a superposition of a number of sinusoidal waveforms. The algorithm uses a single transient input to test for multiple specifications at a time. This is a very important point for reducing the test time; only one waveform is required for testing all the specifications. Furthermore, the waveform generator is relatively simple in complexity compared to an arbitrary signal generator.

The DUT example in this paper is a 900 MHz low-noise amplifier (LNA). The test results on this LNA suggest that with our test generation algorithm, it is possible to have high fault coverage at test speeds lower than the nominal operating frequency, and within a reasonable test time. Furthermore, specifications that are typically measured by application of two sinusoids, as of IIP3, are shown to be effectively measured by a single sinusoidal input waveform. As a result, we claim that the algorithm implements a competitive radio-frequency (RF) circuit testing methodology that satisfies the requirements mentioned in the previous section.

There are two key aspects of the algorithm: (i) the use of an optimization method to limit the number of tones and the highest frequency component of the multitone input, and (ii) the use of a controlled experimentation method to explore the parameter space in an efficient manner. These two contributions are summarized in Section IV of this paper.

III. BACKGROUND

Fault-based testing is an interesting alternative to functional testing in the RF domain. In this methodology, the target of test generation is to maximize the difference between the fault-free and faulty circuits. Depending on the application, researchers have employed various types of test inputs. To name a few, in static dc testing [2,3] a dc voltage or current is applied; whereas frequency domain testing [4,5] uses many sinusoidal signals to study the steady-state response of the circuit; transient testing [6,7] applies piecewise linear or multitone voltage waveforms and samples the transient response.

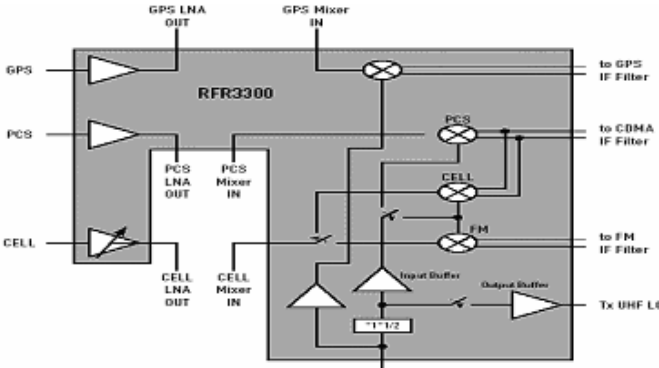


Fig. 1: Qualcomm™ RFR3300™ Dual Band RF to IF Receiver [10]

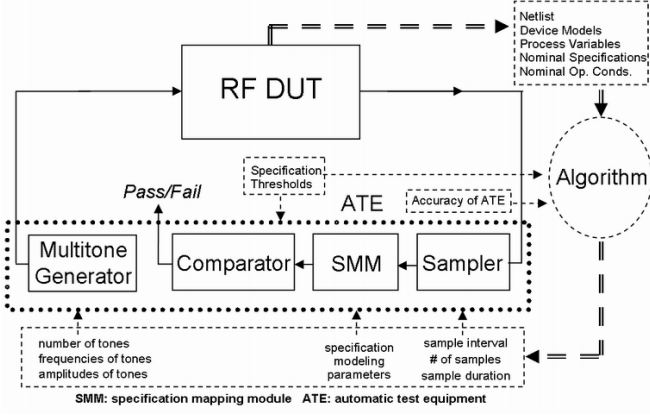


Fig. 2: The proposed test setup for a component within an architecture that allows access to individual components.

In [2-7], the testing method is evaluated in terms of pass-fail analysis with regard to mostly “hard” failures. In [8,9], a new methodology to predict performance parameters directly from transient testing is proposed. In this work we focus on parametric testing of RF amplifiers and carefully analyze the devices that are close to the margin of test acceptance.

IV. APPROACH

This paper investigates the possibility of extending the work in [8,9] by applying multitone waveforms to the input of a radio-frequency device. The waveforms are optimized in terms of a cost function to limit the number of tones, the maximum test frequency, and the total test time by using constrained optimization. As a result, the tests are done at the lowest possible frequency satisfying maximum test time limitations.

A majority of current RF architectures allow access to individual components of the design. Fig. 1 shows the internal architecture of a “dual band RF-to-IF receiver” from Qualcomm™ [10]. The individual pieces of the receiver (LNA, mixer and amplifier, I-Q demodulator, etc.) can be accessed from the external points. Fig. 2 shows the corresponding test setup for a RF device. The automatic test equipment (ATE) generates a multitone transient waveform, which is the input for the RF DUT. The ATE samples the output of the DUT, and the “Specification Mapping Module” (SMM) uses these voltage samples to generate predictions for

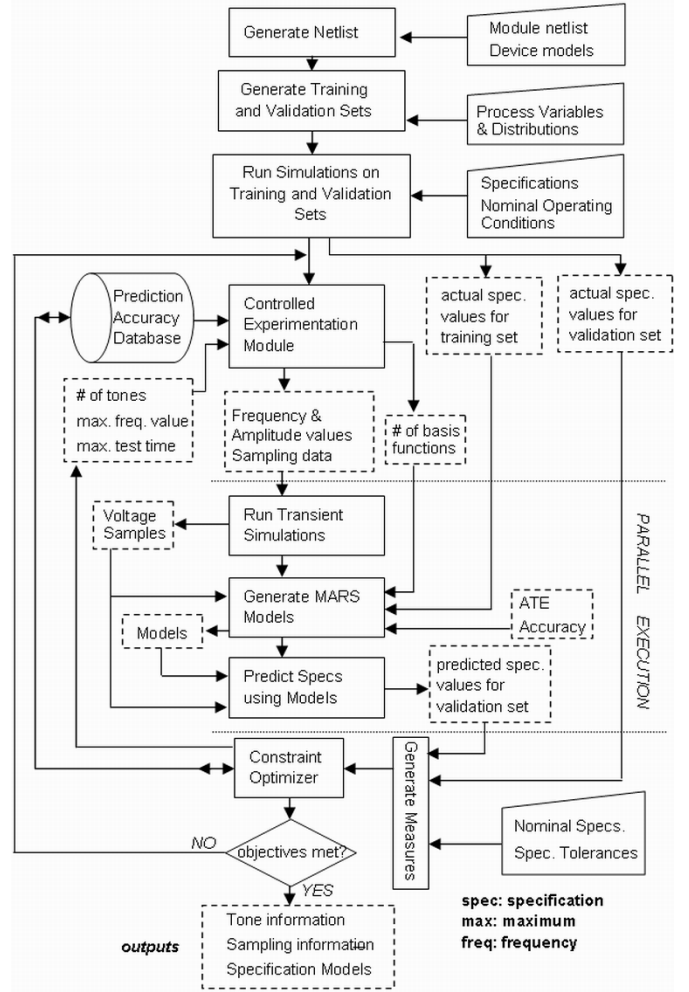


Fig. 3: Control and data flow in the MUSTI algorithm.

multiple specifications of interest at a time [9]. This is a qualitative measure as opposed to deriving hyper-planes [8]. The comparator checks the predictions against specification pass/fail tolerances, and generates an output to identify whether the DUT fails for any one of these specification.

The proposed algorithm, “**M**ultisine **T**est **I**nterface **O**ptimizer” (MUSTI), takes (a) the netlist of the DUT, (b) device models, (c) process variables and distributions of process variables, (d) nominal values of specifications, (e) specification pass-fail tolerances (thresholds), (f) nominal operating frequency of DUT, (g) quality measure for prediction accuracy, and (h) the accuracy of ATE, as inputs; and generates (a) the information necessary to build a multitone input transient waveform, (b) the sampling interval, sampling start time, and number of samples, (c) a specification prediction model for each specification of interest, as the outputs.

Fig. 3 shows the control and data flow for the algorithm. The upper part is computed only once for a given RF device. Two sets of device instances are generated for training and validation purposes using the circuit netlist, device models, and process variable distributions. SpectreRF™ simulator is used to simulate all of these instances at the nominal operating frequency and at the nominal temperature of operation. These

simulations are designed to measure actual specifications of interest for each circuit instance.

The lower part of Fig. 3 describes the iterative optimization loop. First of all, a controlled experimentation methodology proposes a number of possible simulation and modeling sets. Each set is a collection of the following entities: the number of sinusoidal tones, frequency and amplitude of each tone, sampling interval, sampling start time, number of voltage samples, and number of basis functions for a specification model. A number of these sets are selected considering the limits dictated by the constraint optimizer. The first six entities of every set describe a transient analysis in Spectre™, simulations that correspond to the selected sets are run in parallel. The result is a set of sampled voltage values for each simulation. The voltage samples of the training set are used with the number of basis functions, the accuracy of the ATE, and the actual value of specifications to generate a multivariate adaptive regression splines (MARS) [11,12] model for each specification. Then, these models are used with the voltage samples of the validation set to generate predictions of validation set specifications. The measure generation unit compares the predictions with actual values, and applies pass-fail thresholds of the specifications to calculate the accuracy of predictions, which are stored in a database. The constraint optimizer uses this database to select new bounds on number of tones, maximum frequency value, and maximum testing time. If the optimizer satisfies all the objectives, optimization is over; if not, this loop is executed again with the new bounds.

The algorithm for the selection of sinusoidal parameters can be summarized in four steps: Every iteration starts with the selection of an initial vector of n superimposed test frequencies. The next step computes the gradient of the cost function with regard to the amplitudes and frequencies of the sinusoidal waveforms. Then, using the gradient vector, the controlled experimentation module picks the next choice of test frequencies. The module may also merge or split the choice of test frequencies as needed. The algorithm stops if no further improvement in cost is possible; otherwise execution proceeds from the first step with the selection of a new vector of test frequencies.

V. RESULTS

In order to demonstrate the algorithm, the procedure is applied to a 900 MHz low-noise amplifier (LNA). Figure 4 shows the schematic of the LNA with 8 resistors, 5 capacitors, and 2 transistors [13]. The saturation current and the forward gain of the transistors, together with resistor and capacitor values sum up to 17 process variables. Each process variable is assumed to have a normal distribution with

$$3\sigma = nom / 10 \quad (1)$$

where nom is the nominal value for the variable, and σ is the standard deviation. The validation set is a 500 sample random

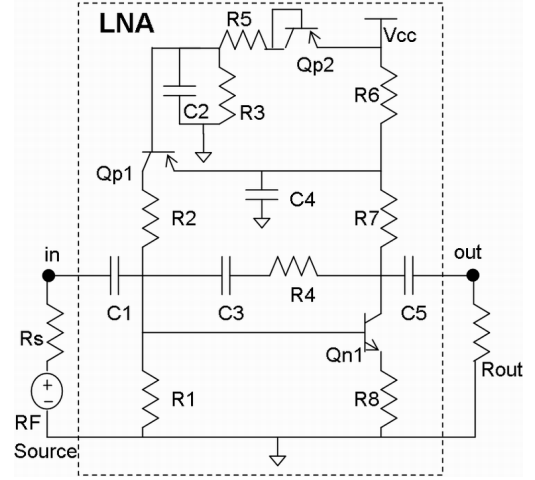


Fig. 4: Schematic of the LNA circuit [13]

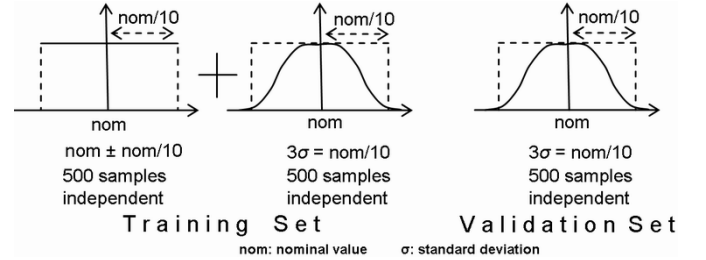


Fig. 5: Distributions for training and validation sets

set with the specified jointly normal distribution. The training set is composed of two parts, the first one is a 500 sample jointly normal distribution; whereas the second part is another 500 sample random set with process variables linearly distributed over the $\pm 10\%$ range around the nominal values. This combination of normal and linear sets provides a large coverage of possible faults, yet preserves the nature of a realistic distribution. The validation and training set instances are generated by the Monte Carlo method. Fig. 5 shows typical distributions for validation and training sets.

The specifications of interest for the LNA example are chosen such that each one emphasizes a different aspect of transient testing. The sample specifications are 1dB compression point (1dB), input referred third order intercept point (IIP3), and the noise figure (NF) at the nominal operating frequency. The 1dB compression point is a good figure of performance for single tone inputs, whereas IIP3 is typically measured by two-tone inputs. Noise figure is highly frequency dependent. Table 1 summarizes the nominal, minimum and maximum values for the distribution of these specifications and the corresponding simulation methods.

The optimizer may use any of the various prediction accuracy metrics. The computation of two of these metrics: the maximum percentage error (mpe) and the root mean square percentage error ($rmspe$) are given in (2) and (3), where $actual$ is the actual value of the specification, $predicted$ is the value predicted by MARS, and rms is the root-mean-square function. The maximum and root-mean-square

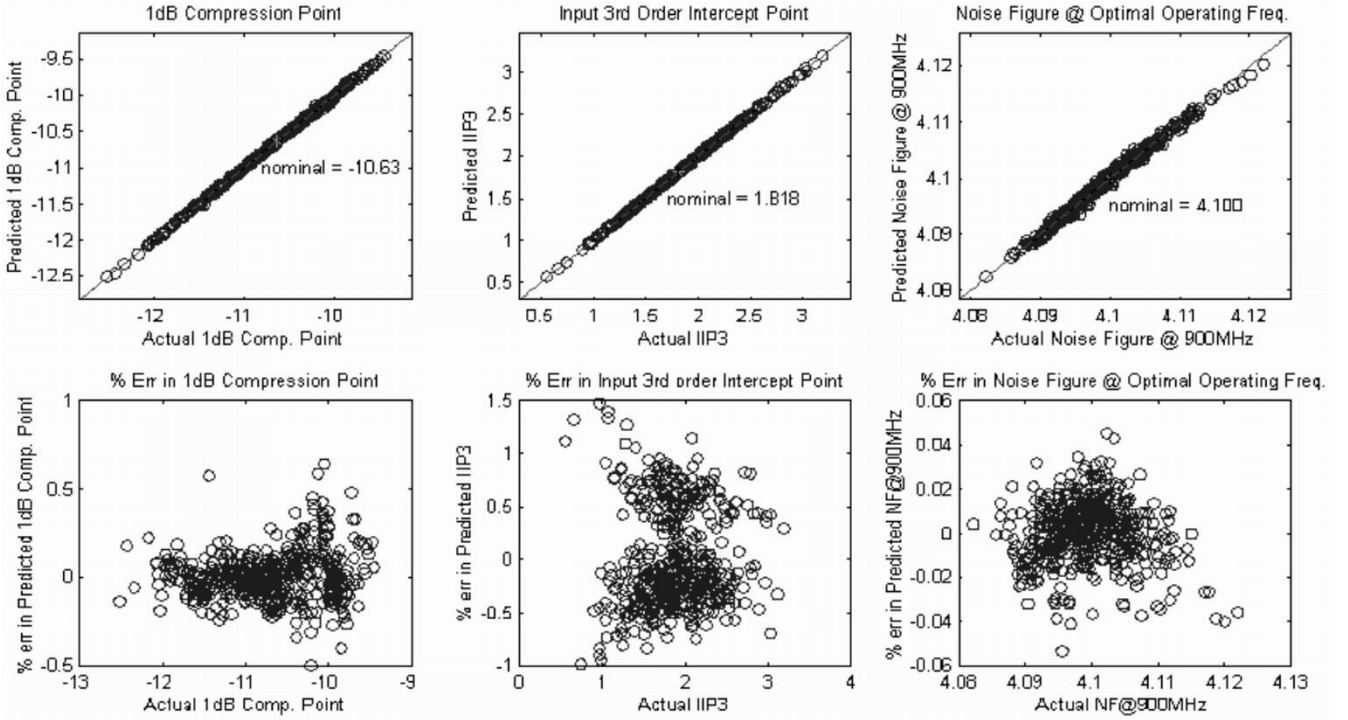


Fig. 6: Single tone test results with 900 MHz input signal.

TABLE I
SPECIFICATION DISTRIBUTION AND ANALYSIS TYPES

Specification	Analyses	Nominal Value	Minimum	Maximum
<i>1dB Comp. Point</i>	pss	-10.63	-13.04	-8.944
<i>IIP3</i>	pss	1.818	0.0234	3.961
<i>NF @ 900 MHz</i>	pnoise	4.100	4.082	4.122

pss: periodic steady state pnoise: periodic noise

TABLE II
VALIDATION SET DISTRIBUTIONS WITH RESPECT TO PASS-FAIL METRICS

Specification	Pass-Fail Threshold	Fail Perc. (in %)	Validation Set Error Tolerance Range from Misclassification (in % of Actual)			Faulty Instances Error Tolerance Range from Misclassification (in % of Actual)		
			min	mean	max	min	mean	max
<i>1dB C. P.</i>	-11.8	5	0.0840	10.9	24.9	0.0965	1.66	5.75
<i>IIP3</i>	1.17	5	0.0914	36.0	110	0.582	20.0	110
<i>NF</i>	4.110	5	0.0002	0.2728	0.6878	0.0002	0.0765	0.2817

functions are computed all over the validation set.

$$mpe = \text{maximum}(|\text{actual} - \text{predicted}| / \text{actual}) \quad (2)$$

$$rmspe = \text{rms}(|\text{actual} - \text{predicted}| / \text{actual}) \quad (3)$$

Mpe is a critical constraint in evaluating the success of predictions. However, due to the nature of the regression algorithm, maximum values of error localize either around the extremums or right around the mean values. Any of these two regions rarely lead to pass/fail misclassifications provided that the prediction error is within some reasonable limit. Our experiments show that an error measure collecting the behavior of the overall specification domain, like the $rmspe$, better fits as an iterative optimization metric.

The main instances of interest are the ones that have specifications close to the pass-fail thresholds. Neither mpe nor $rmpse$ specifically gives an insight on the prediction accuracy around these regions. In order to handle this issue, we introduced quantitative metrics of misclassification into the algorithm. Two metrics quantify the instances that are “bad but classified as good by prediction” and the ones that are “good but classified as bad by prediction”. In our

experiments, the pass-fail tolerances for each specification are arranged such that 5% of the instances in the validation set fail. Table II shows the validation set distributions with respect to quantitative pass/fail metrics; noise figure error tolerance is the smallest hence the most critical one, whereas IIP3 error tolerance is distributed over a wide range, which means that the mpe metric has a rather weak correlation with classification metrics.

Some selected solutions for the MUSTI algorithm are presented in Table III. All parameters for these solutions are the same except for the number of tones and the frequency values of the tones. The first row describes the classical test for IIP3; one of the sinusoids is the nominal operating frequency of 900 MHz, and the other is superposed at 920 MHz. Although the maximum error in IIP3 prediction is close to 10%, none of the instances are misclassified in terms of IIP3. Overall, there is only 1 misclassified instance, which corresponds to 0.2%. The solution in the second row replaces the two-tone input with a single sinusoid at the nominal operating frequency. The resulting prediction accuracy and error distributions are shown in Fig. 6. Maximum percentage error metrics are far better pulling the IIP3 error below 1.5%. The percentage of misclassified instances increases only by

TABLE III
SELECTED SOLUTIONS FOR MUSTI ALGORITHM

# of Tones	Frequency Values	Maximum Percentage Error			# of Should-Pass But-Failed			# of Should-Fail But-Passed			Total # of Misclassified (% out of 500 samples)
		1dB	IIP3	NF	1dB	IIP3	NF	1dB	IIP3	NF	
<i>Two tones</i>	900MHz & 920MHz	1.44	9.75	0.04	0	0	0	0	0	1	1 (0.2%)
<i>Single tone</i>	900 MHz	0.84	1.40	0.08	0	0	2	1	0	1	3 (0.6%)
<i>Single tone</i>	868 MHz	0.56	1.41	0.05	0	0	0	1	0	0	1 (0.2%)
<i>Single tone</i>	411 MHz	0.42	1.69	0.06	0	0	1	1	0	1	3 (0.6%)
<i>Single tone</i>	7 MHz	9.57	5.38	0.17	1	0	2	0	0	3	6 (2.0%)

0.4%. At an even lower frequency of 868 MHz, the misclassification is as low as that of a two-tone sinusoidal input, and the maximum percentage errors get smaller. This is a remarkable point in the sense that our algorithm generates the same fault coverage as a two-tone signal using only a single tone, the frequency of which is lower than the nominal operating frequency, and also provides lower maximum error values. The fourth solution performs almost as good as the second one at a frequency value less than half of the nominal. This is also significant in the sense that, our algorithm cuts the maximum frequency requirement of the ATE by more than 50%, if a 0.6% misclassification is acceptable. Note that it is possible to set the test limits in such a way that all bad ICs are always classified as bad but a few good ICs are rejected [14].

Our experiments show that there is a trade off between the specification coverage and minimum possible frequency value. The fifth solution shows that at a frequency two orders smaller than the nominal operation, the correct classification percentage for 1dB compression point and IIP3 are still high, whereas a misclassification of 2.0% is seen for the noise figure specification. Clearly, significant reductions on ATE complexity are possible using our proposed test approach.

VI. CONCLUSION AND FUTURE WORK

The case studies above suggest that our algorithm can provide a tailored solution to the test problem at hand. The algorithm is flexible in the sense it generates the optimum solution defined by the objective function of the optimizer unit. As a result, the optimal multisine test is a powerful test approach that provides high fault coverage at speeds lower than the nominal operating frequency, easing the need for complex ATE requirements. Furthermore, it reduces the total test time by covering multiple specification tests concurrently.

Currently we are applying the test methodology to embedded analog/RF parts in systems-on-chips, and investigating BIST/DFT methods for the same.

REFERENCES

- [1] S. Ozev, C. Olgaard, and A. Orailoglu, "Testability implications for low-cost integrated radio transceivers: a Bluetooth case study," in *Int. Test Conf.*, November 2001.
- [2] L. Milor and V. Viswanathan, "Detection of catastrophic faults in analog integrated circuits," *IEEE Trans. Computer Aided Design*, vol. 8, pp. 114–130, 1989.
- [3] G. Devarayanadurg and M. Soma, "Analytical fault modeling and static test generation for analog IC's," in *Int. Conf. Computer Aided Design*, 1994, pp. 44–47.
- [4] N. Nagi, A. Chatterjee, A. Balivada, and J. A. Abraham, "Fault-based automatic test generator for linear analog devices," in *Proc. Int. Conf. Computer Aided Design*, 1993, pp. 88–91.
- [5] M. Slamani and B. Kaminska, "Multifrequency analysis of faults in analog circuits," *IEEE Design Test of Computers*, pp. 70–80, 1995.
- [6] S. J. Tsai, "Test vector generation for linear analog devices," in *Proc. IEEE Int. Test Conf.*, 1991, pp. 592–597.
- [7] S. D. Huynh, S. Kim, M. Soma, and J. Zhang, "Automatic analog test signal generation using multifrequency analysis," *IEEE Trans. Circuits Syst.-II*, vol. 46, pp. 565–576, 1999.
- [8] P. N. Variyam, S. Cherubal, and A. Chatterjee, "Prediction of analog performance parameters using fast transient testing," *IEEE Trans. On Computer-Aided Design of Integrated Circuits and Systems*, vol. 21, no. 3, pp. 349–361, March 2002.
- [9] P. N. Variyam, S. Cherubal, and A. Chatterjee, "Specification driven test design for analog circuits," U.S. Patent application serial no. 09/575488.
- [10] Qualcomm™ CDMA Technologies, "RFR3300™ RF-to-IF receiver," Product Specification Sheet [Online]. Available: <http://www.cdmatech.com/solutions/pdf/rfr3300.pdf>
- [11] J. H. Friedman, "Multivariate adaptive regression splines," Stanford Linear Accelerator Center, Stanford, CA Rep. SLAC PUB-4960, 1990.
- [12] C. Y. Chao, and L. S. Milor, "Performance modeling using additive regression splines," *IEEE Trans. On Semiconductor Manufacturing*, vol. 8, no. 3, pp. 239–251, August 1995.
- [13] Cadence Design Systems Inc., "Affirma RF Simulator (SpectreRF) User Guide," section 6, pp. 4, December 1999.
- [14] S. Bhattacharya, and A. Chatterjee, "Wafer probe and assembled package test co-optimization for minimal test cost," *Proceedings of International Mixed Signal Test Workshop*, June 2002.