Low Cost Test of Embedded RF/Analog/Mixed-Signal Circuits in SOPs

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Abstract: Increasing levels of integration and high speeds of operation have made the problem of testing complex systems-on-packages very difficult. Testing packages with multi-gigahertz RF and optical components is even more difficult as external tester costs tend to escalate rapidly beyond 3 GHz. The extent of the problem can be gauged by the fact that test cost is approaching almost 40% of the total manufacturing cost of these packages. To alleviate test costs, various solutions relying on built-off test (BOT) and built-in test (BIT) of embedded high-speed components of SOPs have been developed. These migrate some of the external tester functions to the tester load board (BOT) and to the package and the die encapsulated in the package (BIT) in an "intelligent" manner. This paper provides a discussion of the emerging BOT and BIT schemes for embedded high-speed RF/analog/mixed-signal circuits in SOPs. The pros and cons of each scheme are discussed and preliminary available data on case studies are presented.

Index Terms: SOP testing, analog system testing, built-in testing, digital system testing, automatic test equipment, design for testability, manufacturing testing, self-testing, built-off testing.

1. Introduction

Integration is being defined at a new level, thanks to systems-on-packages (SOPs). These systems bring together not only analog and digital subsystems, but also radio frequency (RF) components as a means of high-bandwidth communication, optics as the media for multi-gigahertz data transfer and micro-electro-mechanical-systems (MEMS) as an interface with the outer world. The design of such

systems makes use of many advantages which are not present in the traditional design flow. Compactness and uniformity of the medium enclosing these systems dictate shorter datapaths and smaller parasitics, hence increase the speed and bandwidth of subsystems communication far beyond classical databuses. Also, the designer is no longer limited with the discrete properties of passives, but can make use of embedded passive components tailored specifically to the application. Furthermore, SOP versions of sensor-processor, actuator-driver and electrical-optical subsystems benefit from increased bandwidth, absence of package-to-package parasitics and lower power consumption when compared to traditional interfaces.

Testing of these complex SOPs proceeds in two phases: (a) verification testing and design debugging and (b) manufacturing test. In (a), tests are conducted on a few prototype samples to ensure the correctness of the design and viability of the manufacturing process. The design verification procedure consists of application of a set of "verification tests" followed by design diagnosis. If necessary, the design is altered, new prototypes are built and a new set of tests are applied until eventually a "perfect" design is obtained [1][2]. Following design debugging, manufacturing test is performed. Hence, the goal is to identify SOPs that are defective through application of tests during volume production. The defective SOPs are due to manufacturing process variations and manufacturing process imperfections. The cost of production test is very important as this is a recurring expense for every part that is manufactured and is the primary focus of this paper.

A typical SOP encapsulates many of its internal functions and production test is performed by application of test signals to the SOP under control of external automatic test equipment (ATE). The key problem is that the external ATE does not have direct access to all the internal embedded functions of the SOP. It may be possible to route some of the internal electrical signals out of the package to the external tester; however, these internal signals operate at frequencies that cannot be observed directly by an external tester due to the frequency limitations of the encapsulating package and lower speed of external I/O. A similar speed and integrity concern is applicable to validating the subcomponents of the system. While traditional systems have test nodes to individually verify the operation of their subsystems, a classical test

approach to SOP suffers from limited controllability and observability of its subsystems. Furthermore, the system specifications "guaranteed by design" depend on validation of associated subsystem specifications, which may no longer be accessible in a SOP configuration. This proposition is especially important for embedded passives [47] constituting a part of the package itself.

Consequently, the call for a testable SOP results in a conflict of interest between the degree of integration afforded by the design process and the level of testability achievable by an external tester. A viable solution is to place the ATE functionalities in close proximity of the SOP module to be tested. This improves the test-access speed, minimizes test signal degradation, and increases controllability and observability of the signals internal to the DUT. One such candidate is the load board itself, where the test functions are migrated from the external tester to the additional circuitry built around the system-under-test. The additional circuitry retains the ability to apply high-speed stimulus to the system-under-test and capture the high-speed test response, which, otherwise, are degraded by the cable parasitics of the low-bandwidth external ATE [2]. The resulting solution, called built-off test (BOT), presents a low-cost alternative to the prohibitive cost of a classical ATE. The other alternative, built-in test (BIT) pushes the external tester functionality into the package and even into the bare dies wherever possible and is consequently a much more aggressive version of built-off test.

Note that without built-off test and built-in test very high performance SOPs may not be economically testable. This is because the cost of external test equipment for test signal speeds in excess of 1 GHz is very prohibitive. However, multigigahertz system designs are now becoming quite routine for high-bandwidth communications. The test economics is greatly improved by having high speed test functions on the load board (BOT) or the SOP itself (BIT) augmented with low-bandwidth communication with a (low-speed) external tester. This allows very high speed systems to be tested with a low-cost external tester without loss of test quality.

The rest of the paper is organized as follows: Section 2 describes built-off test and built-in test in detail and lists the pros and cons of each approach. Section 3 revisits fault models described in the literature and defines the notion of test quality for a test methodology. Sections 4 and 5 review the approaches in mixed-

signal and RF test literature that are applicable to built-off and built-in test of SOPs. Section 6 covers extensions of these approaches to testing of analog and RF modules in SOP and Section 7 discusses high-speed digital test of SOPs. Conclusions are presented in Section 8.

2. Built-Off Test and Built-In Test

While migrating external tester functions to the proximity of the device-under-test (DUT) there are two different possibilities: (1) the DUT is considered as an end product without having dedicated test functionality internal to the device and, hence, the test support circuitry is built around the device, or (2) the test support functions are implemented within the device as an integral part of it. The first approach, built-off test, is suitable for applications where the internal design of the DUT can not be modified for test purposes and the package itself does not constrain the speed of the test signals that can be applied to the DUT. The second approach, built-in test, is more of a design-for-test (DfT) methodology. The support functions are implemented within the same package or even in the same chip area. In this approach, the device is modified to incorporate some additional functions within the chip by using dedicated test circuitry [48][49][50][51] and by reusing components [53] such as analog-to-digital (ADC) and digital-to-analog (DAC) converters already available at the system level. The introduction of test circuitry into the device may violate original design constraints, e.g. device matching, parasitic loading, etc, and, as a result, additional design iterations may be needed during system design. Consequently, built-in test is feasible only when it can be integrated into the system design flow.

Irrespective of whether built-in or built-off test is used, the load board is a necessary component in a production test environment and typically routes the signal from (to) the test-head of the external ATE to (from) the DUT. Figure 1(a) shows the role of a load board in a high-end conventional ATE environment. In this environment, the load board contains a low-parasitic socket to hold the DUT, power and ground planes, signal traces and switches/relays to multiplex external tester resources. The entire test stimulus is generated by the external tester, and the DUT response is directly relayed to it. High-bandwidth data transfer is performed at the operation speed of the DUT. In built-off test, this channel is replaced by a

low-bandwidth connection, which is utilized to send test control signals as well as low-speed test stimulus and also to receive compact signatures extracted from the DUT response. The high-speed test stimulus and response signature generation is handled at the load board by means of customized signal generators, samplers, converters, modulators, demodulators, multiplexers and demultiplexers. Modems convert the low-speed stimulus coming from the external tester into high-speed stimulus required by the DUT, similarly the response is downconverted. Alternatively, the test stimulus can be generated on the board and response can be compressed into a signature by samplers and converters. Figure 1(b) depicts a general built-off test strategy. Built-off test implements complex test signal generation and test signal modulation schemes without employing expensive 'feature-enriched' testers at the expense of higher load-board manufacturing cost in production test. The high-speed test signal processing is all done on the load board itself under external tester control. The tester employed is typically low-cost with low-speed test data transfer (digital and analog) to and from the load board.

Built-in test (Figure 1(c)) pushes the tester functions into the DUT in order to overcome two main issues in testing: excitation of the DUT and the propagation of the response to an external "test" node. As the complexity and integration of SOPs increase, both issues become harder to tackle, and the test paradigm shifts to solutions where DfT [19][20][21] is employed to improve the controllability and observability of internal nodes [42][41]. IEEE 1149.1 (JTAG) [44] boundary-scan standard provides an effective means for test-access to internal modules of the DUT [43] for testing static faults in digital ICs; however, its JTAG counter part in mixed-signal testing, the IEEE 1149.4 standard [46], is limited by its low bandwidth [45]. Hence, built-in test of analog, RF, and mixed-signal electronics still presents the following major challenges:

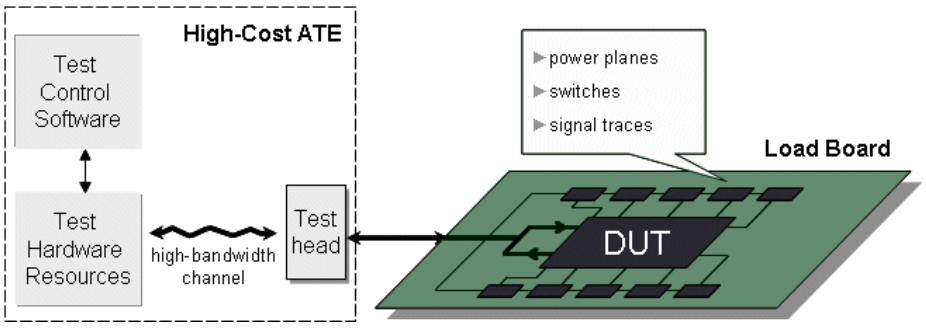
1. On-chip generation of high-speed test stimulus using low-cost hardware,
2. High-speed on-chip response acquisition followed by analysis or response compaction.

In built-in test, low-speed communication takes place between the external tester and the built-in circuitry inside the DUT. This media is used to start or stop a test or run status-checking commands, while the built-in test circuitry performs the rest of the testing "in-situ". Although this approach addresses the

tester cost and test access limitation problems, large chip-area taken by these circuits, especially in mixed-signal testing, makes it often uneconomical for testing all chip functionalities "in-situ". With the evolution of highly integrated systems such as SOPs, this area overhead is of less concern thanks to the reuse of already embedded components such as DACs, ADCs and on-chip Digital Signal Processors (DSP).

The embedded functions in built-off and built-in tests carry different levels of intelligence. They can be implemented in such a way that they create all necessary test vectors and analyze the DUT response on demand, generating a conclusive result about the state of the device. The resulting approaches "built-off self-test" (BOST) and "built-in self-test" (BIST) are complete and independent of any external tester help; however, they may require enormous processing power especially when analog and RF components are to be tested. Such components are more likely to benefit from a low-speed low-pin-count external tester, which analyzes the response signature and generates the test control and low-speed excitation signals. In this kind of "less intelligent" support, the external tester can also be utilized to test the operation of built-off or built-in test components before testing the DUT, and provides flexibility when additional tests are required in the production line. On the other hand, a true "self-test" is not limited to the production line, since it can be applied throughout the life time of the device periodically or right before it is turned on. This may be an important criterion for critical systems that are likely to detoriate over time, such as in space applications. Such schemes are more likely to be implemented as built-in test since built-off test requires a load board.

(a)



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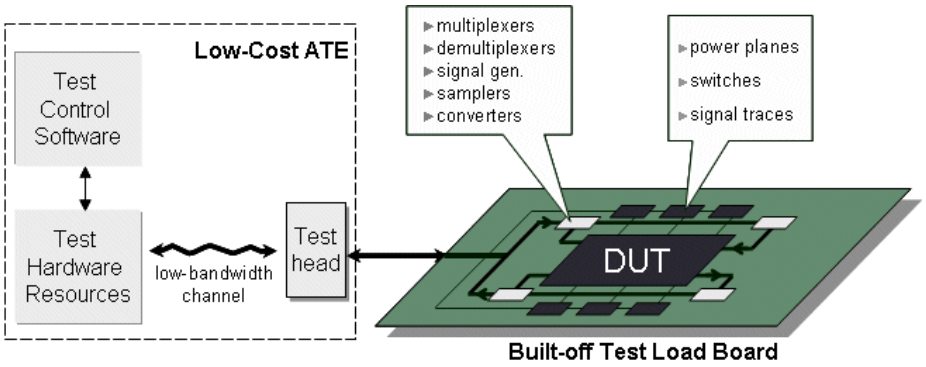

(c)

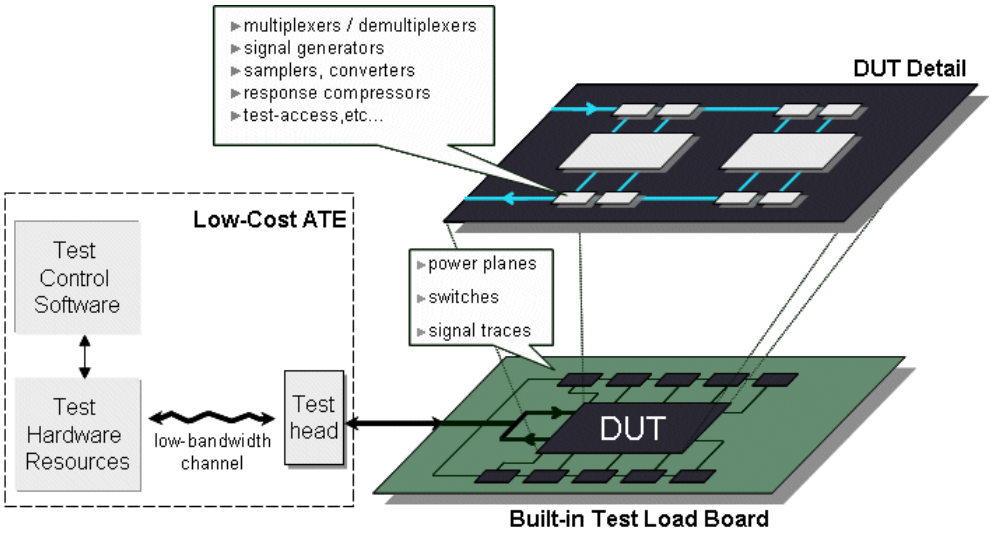

Figure 1. (a) Load board in a high-end conventional ATE environment (b) general built-off test strategy (c) general built-in test strategy

3. Fault Models and Test Quality

Failures in analog and mixed signal circuits are broadly classified into two categories [1]: catastrophic, where the circuit fails to operate correctly due to internal manufacturing defects like shorts and opens; and parametric, where one or more specifications of the device deviate from the respective design values due to random variations in the manufacturing process. Defect oriented tests (DOT) [2] are based on finding a suitable test signal in order to detect the presence of catastrophic failures using different automated fault simulation and test generation techniques [3][4][5][6][7]. The specification oriented tests (SPOT) [8][9][10][11][12] are concerned with a direct or indirect measurement of the specification on the device data sheet. Under these two categories, test quality metrics are defined so that the effectiveness of a test methodology can be evaluated and that of various test methodologies can be directly compared for a given DUT.

While fault coverage [62] is an accepted test quality metric used for testing digital circuits, its extent and meaning in analog domain is not completely clear in literature. Often the analogy between stuck-at faults in digital circuits and opens/shorts in analog domain is carried too far into the fault coverage of an analog test and is defined as the percentage of potential shorts and opens the analog test can detect. However, catastrophic failures that result in significant performance loss of the DUT are detected by simple tests. In reality, the effectiveness of an analog test methodology is largely dictated by its ability to detect parametric failures of the DUT, where performance deviates by a small amount from the nominal. These parametric failures are more likely to occur than catastrophic ones, but are harder to detect than the latter. Furthermore, the meaning of parametric fault is not clearly defined, since any excess variation in a component's value, although considered as a fault, may have little impact on the device specifications. If the test methodologies geared toward increased fault coverage, especially DOT oriented ones, base their evaluation on parametric faults of individual components, they will eventually end up compromising yield coverage, the probability that a fault-free device passes the test [14].

In built-in test applications, an important test quality metric is the area overhead, the percentage of extra area introduced by tester related electronics. It is a major concern for practical implementations, since this

extra area does not add any value after the device passes the production test barrier. This argument, however, is not valid for some built-in self-test solutions, in which the test can be applied throughout the life-span of the product. Often the area overhead is over-emphasized when compared to the yield coverage in the qualification of built-in test methodologies. However, only the joint figure of these two metrics can define the effective wafer area dedicated to the product.

Any system-level test methodology needs to ensure that all the specifications in the device data-sheet are verified in production before the device is shipped to a customer. One possible approach to achieve the above is testing every individual sub-module of the device followed by testing of the proper connectivity of the sub-modules inside the SOP. In effect, this approach breaks down the system testing problem into many smaller module level testing problems. Although this approach requires physical test access to the individual internal sub-modules for module-level testing, it is often more effective than end-to-end system level test in terms of both the production test feasibility and the test cost. As an example, for wireless transceiver application, the testing of RF signal blocks, IF signal blocks and Codec blocks can be performed independently and the connectivity of the concerned modules can be verified subsequently to qualify the devices as "good" or "bad" in production test.

However, in such bottom-up test procedures, algorithms for relating the individual submodule test responses to the (system level) test specifications of the SOP must be devised to aid in the pass-fail decision making process. *The key is that any circuit, submodule or system-level failure that causes any of the system-level test specifications of the SOP to be violated is defined to be a "fault"*. Any "correct" test methodology must be designed such that it can detect even the smallest of manufacturing defects that can result in such a fault. If no suitable algorithms for determining the system-level test specification values from the SOP submodule test responses can be found, then the only recourse is to directly measure the relevant test specifications at the system level. In general this is more expensive than running submodule level tests. A typical example is testing of the input referred third order intercept point (IIP3) specification of circuits exhibiting non-linear behavior. Measuring end-to-end IIP3 requires high-performance

(expensive) measurement instruments. However, if it can be inferred from the results of submodule test then it can be performed using a simpler setup. This is the subject of ongoing research [58].

4. Direct Measurement of Specifications Using Dedicated Circuitry

In traditional production test approach for testing of analog and mixed signal circuits, the functional specifications are measured using the appropriate tester resources and using the same kind of test stimuli and configuration with respect to which the specification is defined [40], e.g. multitone signal generator for measuring distortion, gain for codec, ramp generator for measuring INL, DNL of ADCs and DACs, and so on. The measurement procedures are in agreement with the general intuition of how the module behaves and, hence, the results of the measurement are easy to interpret, in contrast to the concept of 'alternate test' [16] (described in Section 5).

In the direct measurement approach using built-in test, the external ATE functionality is designed inside the DUT for applying appropriate test stimuli and measuring the test response corresponding to the specification. In [63], adjustable delay generators and counters are implemented next to the feedback path of a PLL to measure the RMS jitter. Since the additional circuitry does not modify the operation of the PLL, the same built-in test circuitry can be employed on-line. [63] also discusses different ways to measure properties like loop gain, capture range and lock-in time by modifying the feedback path to implement dedicated phase delay circuitry. All these built-in test components are automatically synthesized using the digital libraries available in the manufacturing process. This kind of automation provides scalability and easy migration to different technologies. The approach of [64] is similar to this approach in the sense that the extra tester circuitry is all-digital and can be easily integrated into an IEEE 1149.1 interface. In this paper, the built-in test reuses the charge pump and the divide-by-N counter of the PLL in order to generate a defect-oriented test approach, which can structurally verify the PLL. While [63] can also be implemented as a built-off test, [64] is limited to built-in test since a multiplexer must be inserted into the delay sensitive path between the phase detector and the charge pump. Since both examples employ all-digital test circuitry, their application is limited to few analog components like PLLs, where digital control is possible.

The works of [53], [54], [57] and [56] attempt to implement simple on-chip signal-generators and on-chip test response data capture techniques for testing the performance of high-frequency analog circuits. The communication between the built-in test hardware and external world takes place through a low frequency digital channel. In particular, [56] measures the spectral content of the test response using direct down conversion of RF test stimuli and test response waveforms. Although the chip-area taken by additional test circuitry is still a concern, it shows the feasibility of using built-in test for measuring performance of high-frequency embedded analog/RF blocks in-situ.

With regard to built-off test, direct measurement techniques for different classes of analog circuits are discussed in [2]. The circuitry for measuring one test specification is reconfigured to measure another using a set of relays and switches on the DUT load board. Typically, the load board test circuitry is designed with the DUT designer's input, unlike the method presented in [61], and takes several weeks to debug.

Although the direct measurement procedures are conceptually simple, this approach has inherent drawbacks as described below:

1. Multiple specification measurements requires different kind of resources, which are difficult to build either "on-chip" or on the limited load board are due to high area overhead.
2. Longer over-all test time is required since measurement of multiple specifications can not be performed simultaneously.

As a result, direct measurement techniques are not suitable for built-in test as test resource requirements are very high, associated built-in test hardware overhead costs are prohibitive, and the time necessary for testing each specification separately increases the overall manufacturing cost.

5. Alternate Testing Methods for Mixed-Signal/RF Circuits

As the cost of conventional test remains a prohibitive factor for testing of analog and RF circuits, the concept of alternate test was proposed in [15], [16] and [17]. The underlying principle of alternate test, also discussed in [13] and [14] in a different context, is described below. The variation of any process or circuit

parameter, such as width of a FET, value of a resistor, etc., in the process or circuit parameter space P affects the circuit specification S by a corresponding sensitivity factor. If M is the space of measurements (amplitudes values of subsystem output spectrum, for example) made on the circuit under test, the variation in the parameters also affects the measurement data in the measurement space M of the circuit by a corresponding sensitivity factor. Figure 2 illustrates the effect of variation of one such parameter in P on the specification S and the corresponding variation of a particular measurement data in M. Given the parameter space P, for any point in P, a mapping function (nonlinear) onto the specification space S, $f: P \rightarrow S$, can be computed. Similarly, for the same point, another mapping function (nonlinear) onto the measurement space in M, $f: P \rightarrow M$, can be computed. Therefore, for a region of acceptance in the circuit specification space, there exists a corresponding allowable "acceptable" region of variation of parameters in the parameter space. This in turn defines a region of acceptance of the measurement data in the space M. A circuit can be declared faulty if the measurement data lies outside the acceptance region in M.

Alternatively, as shown in [16] and [17], a mapping function $f: M \rightarrow S$ can be constructed for the circuit specifications S from all the measurements in the measurement space M using nonlinear statistical multivariate regression. Given the existence of the regression model for S, an unknown specification of a DUT can be predicted from the measured data. In the proposed alternate test approaches, Multivariate Adaptive Regression Splines (MARS) [60] were used to construct the regression models [38][39] and estimate the test specifications of the subsystem from the frequency spectrum of the test response waveforms. The objective of the alternate test methodology is to find a suitable transient test stimulus and to predict circuit specifications accurately from alternate test response. Different type of test stimuli, viz. (1) piecewise linear [39], (2) multitone sinusoids [58][65], (3) digital pulse trains [52] are used in different cases. The methods are used successfully to test op-amps [39], low-frequency filter circuits [39] and high-frequency RF modules [58]. In particular, using digital pulse train generated from linear feedback shift registers (LFSR), as in [52] and [55], facilitated built-in test approaches due its low area overhead. In fault diagnosis, which is another key problem in testing SOPs, symbolic formulation and analysis

[22][23][27][28][29] are usually not possible. However, alternate test generation based diagnosis schemes demonstrated in [24][25][26] can be applied to solve the fault diagnosis problem.

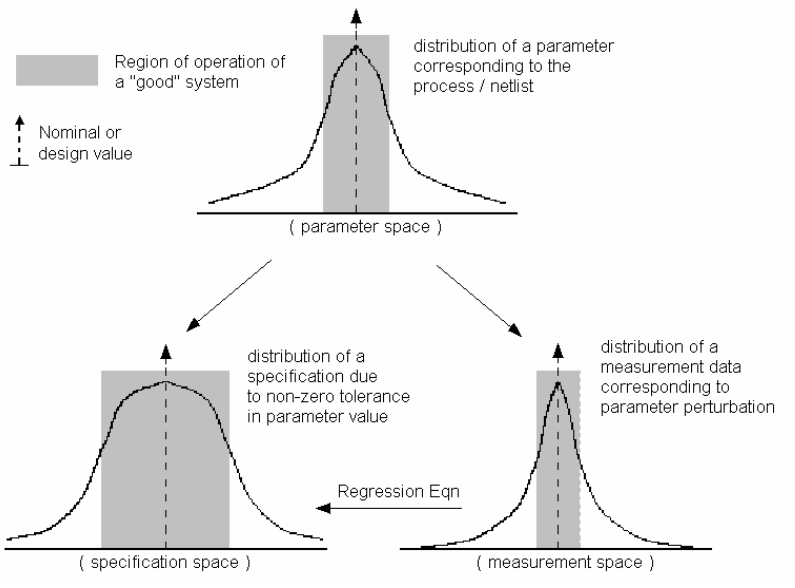

Figure 2. Variation in process or circuit parameter and its effect on circuit specification and test response measurement.

Recent literature addresses applications of alternate test to RF components. In [59], the load board modulates the baseband test stimulus provided by a low-cost tester and uses the resultant RF signal to stimulate a low-noise amplifier (LNA). The response is downconverted on the load board and low-pass filtered to generate a signature that can be transferred to the tester through a low-bandwidth channel and analyzed using alternate test principles. The application follows the generic modulator based built-off test scheme in Figure 3. An alternative to this scheme is using a simple signal generator that can be implemented on the load board. [65] describes an alternate test generation methodology that seeks an optimal superposition of sinusoids. Simulation results suggest a single sinusoidal, which has two orders of magnitude smaller frequency than the nominal, can be used to excite an RF LNA, and the response can be sampled with load board capabilities. A different alternate built-off test approach is reported in [66], which

employs the bias control voltage of a RF power amplifier as the test stimulus, and measures the bias current to predict critical components specifications like gain, noise figure and power efficiency. The use of current measurements in response acquisition proposes a noninvasive alternative to voltage measurements in RF applications where tapping into sensitive nodes is prohibitive.

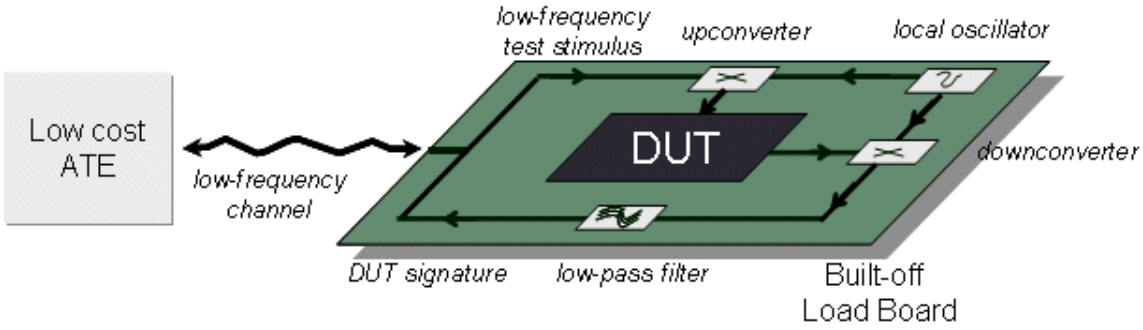

Figure 3. Modulator/demodulator based built-off test scheme

In [55], another version of built-in test scheme is proposed, which deviates from 'self-test' paradigm in order to minimize additional test related hardware put inside the chip and to reuse the existing test-hardware already present for testing digital section of the system IC. Unlike built-in test schemes discussed in [49], [50], and [51], the DUT response is analyzed externally inside a low-cost ATE. Since the DUT test response waveform is transformed to a digital bit-stream and scanned out through the scan chains of the digital cores, the approach can be integrated with IEEE 1149.1 based scan structure. Hence, the proposed technique attempts to solve the limited test access problem for embedded analog modules in system ICs to a large extent and can be used for testing the embedded passives. The test response waveform is reconstructed for analysis in the external tester, and from the reconstructed test response waveform, the DUT's specifications are predicted using the regression analysis discussed in alternate test.

In another kind of built-in test approach, the circuit topology is changed using additional circuit elements to make the circuit behave differently from that it is designed for and this modified functionality is usually easy to measure in production test environment. The catastrophic faults that make the original circuit performance to fail, also causes the reconfigured circuit 'performance' to deviate. The latter

performance deviation is measured during production test and pass/fail decisions for the original circuit are made. Oscillation based tests (OBT) [33][34][35] acts on the above principle, which reconfigures analog filter circuits into oscillators using additional feedback components. This built-in test technique detects catastrophic faults in DUT by measuring the deviation in oscillation frequency and amplitude. In recent years, the above defect-oriented built-in test technique has been integrated with the regression modeling approach commonly used in alternate test and the modified OBT is used for predicting specification of DUT under parametric failure conditions. The modified technique relies on the fact that, the original circuit and the reconfigured circuit share almost all the circuit components and, hence, a direct correlation between the original circuit performance and the modified circuit performance (the latter 'performance' is not a design goal) values can be established when the circuit parameters vary. This correlation is computed using circuit simulation under parametric variations using regression analysis previously used in alternate test. The modified OBT, referred to as predictive oscillation based test (POBT) [36], predicts the performance of the original circuit by computing the above correlation and measuring the oscillation frequency of the modified circuit during test. One inherent drawback in OBT approaches is that very few circuits other than analog filters can be reconfigured into oscillators.

Built-in response acquisition presents a significant problem in testing RF submodules. In mixed signal environments with built-in ADCs, the analog response can be fed into the ADC and scanned out to the external tester in digital form after compaction. However, in RF systems, the inherent ADCs are configured to process near-baseband signals, so their performance is not adequate to process high-frequency passband responses. [67] and [68] tackle this problem by introducing a statistical sampler that compares the analog response with noise. The power spectral density (PSD) of the resultant digital bit stream is a representation of the original PSD with an increased noise floor. [69] extends this methodology by an automatic feature extraction scheme that detects the PSD components above the noise floor introduced by the statistical comparator, and uses these components with a non-linear mapping model to predict device specifications like gain, third order intercept point, noise figure and power supply rejection ratio. This scheme, given in Figure 4, also presents an extension to the alternate test methodology in the

sense that the scheme can compensate imperfect tester conditions simulated with a random fluctuation superposed onto the ideal input stimulus.

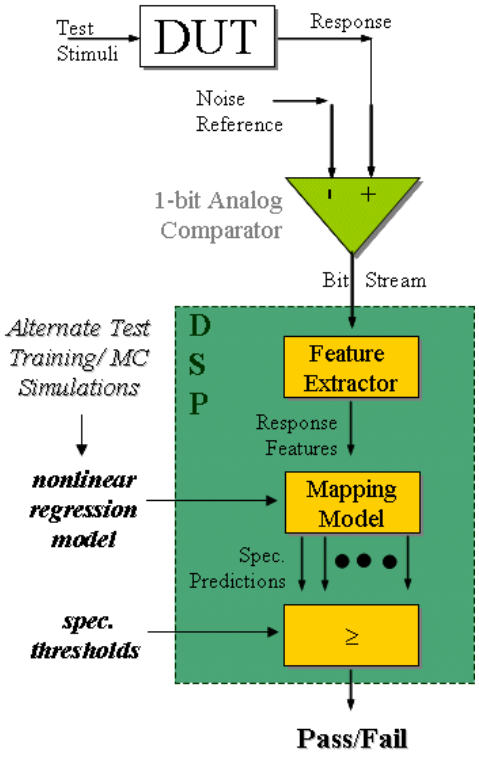

Figure 4. Noise referenced, feature extraction based built-in test scheme.

6. Testing of Analog/RF Modules in Systems on Packages: Direct Measurement or Alternate Testing?

As discussed in the first section and explained later on, SOP requires non-orthodox test methodologies that can keep up with the test access problems amplified by the inherent integration, and do away with the prohibitive cost of high-end external testers. Built-off and built-in test strategies propose a solution to these problems by placing high-bandwidth test access either next to the package or within the package. The SOP test challenge also calls for automated test solutions, which are not only generic enough to cut down custom-test support development cost but also customizable enough to make the test-support financially feasible. This requirement ensures that the turn-around time associated with test generation and test

hardware development is little reflected into the device manufacturing cost. Although different direct measurement based test approaches reviewed in Section 4 propose promising results for stand-alone devices; *their application at a system scale is not feasible due to the need for custom test-support hardware for every embedded module to be tested*. Since they do not provide a generic methodology to handle direct measurement of different specifications, each specification to be tested increases the over-all turn-around time for product development, as well as they increase test area overhead and testing time for every device.

On the other hand, alternate test methodologies reviewed in Section 5 propose generic solutions for embedded analog and RF components; which cover a large range of system components available in SOP, viz. embedded passives, op-amps, filters, LNAs, mixers, power amplifiers, etc. The ability to predict multiple specifications using a single test reduces the test hardware complicity, area overhead and the testing time. Furthermore, statistical sampler based extensions are compatible with applications utilizing digital scan architecture (IEEE 1149.1), since the resultant bit stream can be relayed to the digital signal processors in the package at no additional cost.

Since alternate built-off test methodologies propose a systematic way to handle a large range of specifications and sub-modules, their integration into the product flow does not increase the complexity and cost significantly. Although the load board will be populated with extra components to accommodate test related signal processors, the increase in board design time can be compensated with automation already present in the traditional load board manufacturing flow [61]. The manufacturing cost of traditional load boards are dominated by the quality of the material, many levels of power planes provided and the necessity to use only golden boards, boards that very closely follow the specifications of the original board design. In the case of built-off test, the extra cost of signal processor ICs, their routing and assembly will not be significant when compared to the traditional load board figures. Furthermore, the use of built-off test will benefit from low-end ATEs, which provide two orders of cost reduction compared to high-end ATEs necessary for traditional tests [90][91][92]. This reduction is still one order greater than the manufacturing cost of many typical complex load boards. The only practical limit for load board complexity is the fixed area dictated by the interface of the production testing equipment. *It is important*

that when it comes to testing of very complex systems like SOPs, one of the main problems is feasibility rather than cost [93][94]. As discussed in Section 1, even with high-end ATEs, it is not possible to address bandwidth requirements of such systems. Section 7 further elaborates on feasibility using examples from multigigahertz digital test.

A viable SOP strategy using alternate tests should generate specification oriented tests considering only the components specifications that progressively develop a violation at the system level. The first step will be analyzing the system specifications to break them down into related component specifications; this process is usually a part of the system design hence it will not induce further effort. Then, all related specifications can be tested by a single alternate test per component. Some system level specifications that can not be verified by a collection of individual component performances will further be covered by system level alternate tests. [58] presents an example to this scheme, where system level specifications of RF sub-system of a narrow-band wireless transceiver (Figure 5) are verified by alternate test generated on high-level models of the system. In this example, multi-tone sinusoid stimulus is optimized for the test and test response spectrum is measured for specification prediction. Multiple system specifications, such as gain and IIP3 of the RF subsystem, are simultaneously and accurately predicted using statistical regression. The prediction error in measuring end-to-end specifications is significantly small (within ±1dB) for these high-frequency complex subsystems. High-level modeling speeds up the simulation intensive features of alternate test, which are not feasible for SOPs at the netlist level. Furthermore, the inherent complexity of SOPs makes built-in approaches more favorable than built-off test solutions. On the other hand, a joint built-in/built-off approach can add more value to the package area, where module level access and DSP is handled by built-in tester components while more area intensive tester functions like analog signal generators and modulators/demodulators can be migrated onto the load board.

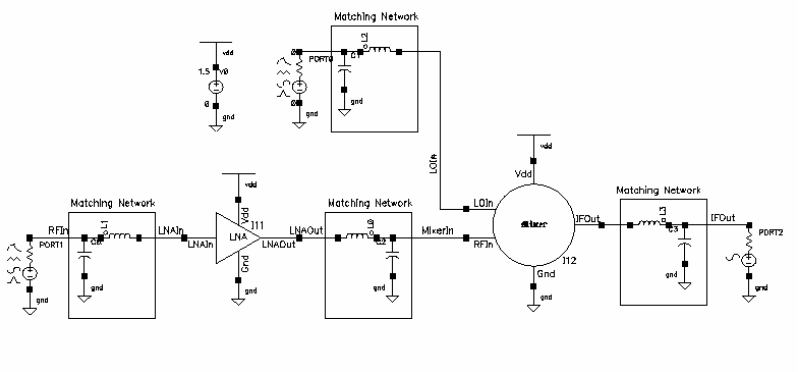

Figure 5. Block level diagram of the RF subsystem under test

7. Multigigahertz Digital Test: Recent Developments

A snapshot of the recent developments in multigigahertz digital testing research can be obtained by examining papers presented at the International Test Conference [70-89]. The objectives for each of these fall into two broad categories: (1) increased test performance, and (2) reduction in test cost. At any given point in time, these two needs tend to have conflicting requirements, so a trade-off or balance between them is usually sought. Still, over time, improvements in both are required. Existing automated test equipment (ATE) is limited to 1 to 1.6 Gbps per channel in most cases. Yet devices must be tested in the 2.5 to 3.2 Gbps range, and occasionally as high as 10 to 12 Gbps. The capital cost of such ATE can exceed several million dollars. That high price is a concern in itself, but it places tremendous emphasis on the need to minimize time on the test system (increase test throughput). The multi-million dollar capital cost translates into significant dollars-per-minute costs on the test floor.

Generally the various trade-offs between performance and cost issues for multigigahertz ATE are discussed in a series of "position papers" [82-89] on the future directions for ATE development. The authors provide various views as to the specifics of how best to balance these seemingly incompatible requirements.

Increased performance, in this context means: (1) higher speeds (multi-gigabit-per-second data rates), (2) better timing resolution and accuracy (picoseconds), and (3) extended functionality and flexibility (to accommodate new device functions and signaling methods). Obtaining higher data rates alone is usually

not the greatest obstacle since the basic technology for achieving higher speeds continues to improve (largely due to reductions in transistor minimum feature sizes). However these same higher speeds greatly impact the need for tighter timing accuracy. So the focus of these recent works tends to be in this area of performance. In some cases new test methods are also required to deal with innovative functions and new signaling conventions such as source-synchronous signaling[80].

The various approaches used to solve the problems of performance and cost for multi-gigahertz digital testing include: built-in test [72,77,78,80,81,82], built-off test [73,76], ATE instrumentation improvements [70,74,82,84,87,88], and interface improvements [71,73,76,79].

The control and/or measurement of jitter at the level of picoseconds is a central issue in many of the recent articles [70,71,72,83,84,86,89]. Since the ATE is normally designed as a synchronous system, it includes its own clock signals that are distributed throughout the test electronics and eventually determine the timing accuracy of the test. At the high data rates jitter contributes a significant fraction of the overall uncertainty in edge placement accuracy, so control of jitter within the ATE itself is a challenge. Likewise, the ability to accurately test for jitter tolerance or jitter characteristics of the DUT output signals is difficult because the accuracy required is comparable to the jitter levels of the ATE itself (on the order of a few to several picoseconds for RMS jitter).

In other works [73,74,76,79,80,81-89], obtaining higher data rates (usually with an emphasis on maintaining or lowering cost) is a main objective. In these efforts all of the component elements in the ATE are considered for possible improvement in order to economically achieve multiple gigahertz test speeds. These include the ATE “pin electronics” (memory, multiplexers, formatters, timing edge generators, clock distribution, input/output buffer/drivers, etc.), the overall ATE architecture itself, the interface between the ATE and the DUT, circuits and methods for handling new signaling standards, and ways to take advantage of built-in self test features of the DUT. In [76] for example, additional electronic multiplexers and high-speed samplers are added to the test interface as illustrated in Figure 6, forming “Driver” and “Receiver” modules. In this example, the multiplexing modules combine signals from a 1 Gbps ATE to form multi-gigahertz (2 to 3 Gbps) test stimuli. An example is shown in Figure 7. In another

example [73], the concept of a "Test Support Processor" is used to create a miniature test module that can provide customized high-speed test signals locally to the DUT during wafer-probe testing (see Figure 8). This minimizes the transmission line lengths so that high-quality signals can reach the DUT multigigabit-per-second rates. An example of the test signals at 5 Gbps is illustrated in Figure 9. A potential advantage of this approach is that it can (in principle) be replicated into an array of miniature testers for parallel multi-gigahertz testing at the wafer level.

In almost all cases, the cost of testing, and specifically the cost of the increased performance required by multi-gigahertz devices is a major issue, and in some it is the primary objective [74,75,82,85,87,88]. As pointed out above, the ATE costs are already high for systems that can perform at about 1 Gbps. Extrapolating to 10 Gbps results in vastly more expensive systems. Therefore innovations are needed for finding ways to obtain the required higher performance without incurring substantial increased test costs.

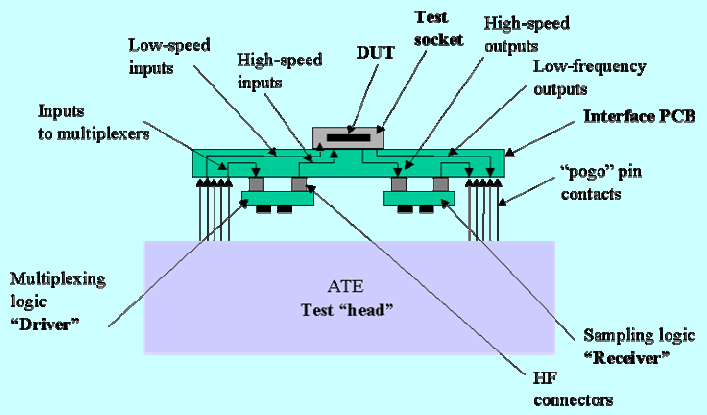

Figure 6. Multiplexing "Drivers" and high-speed sampling "Receivers" at the DUT-ATE interface [76].

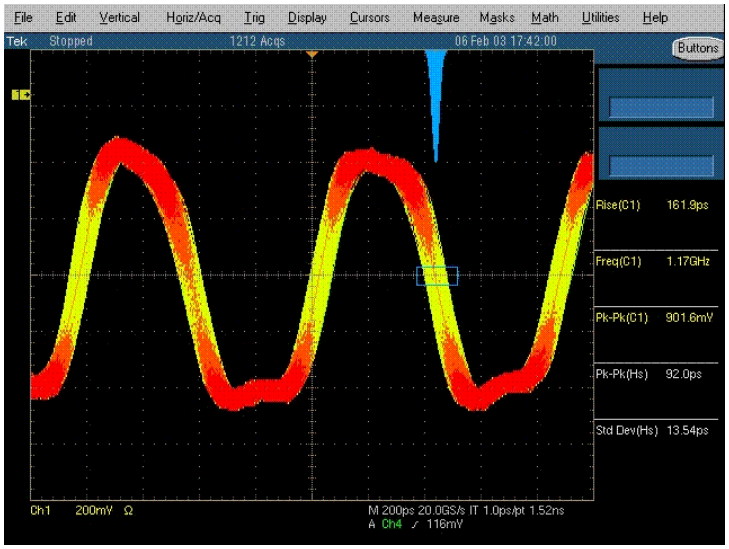

Figure 7. Example 2.5 Gbps signal from the multiplexing Driver module [76].

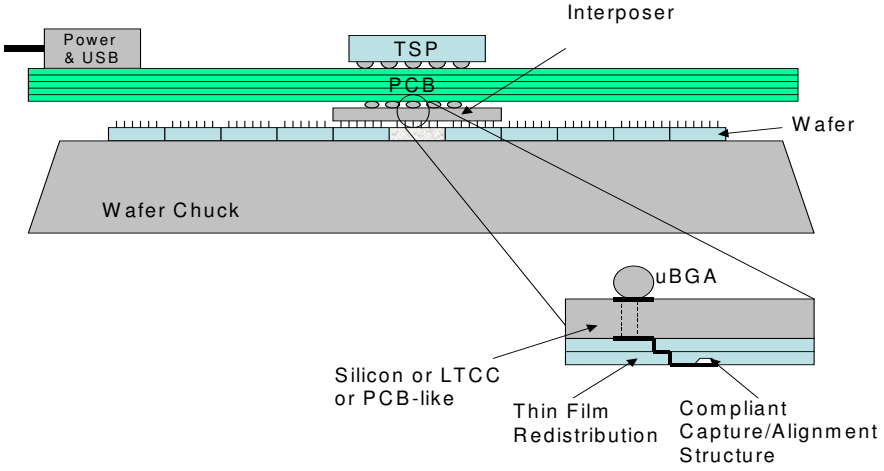

Figure 8. Miniature TSP-based tester in a wafer-probe test arrangement [73].

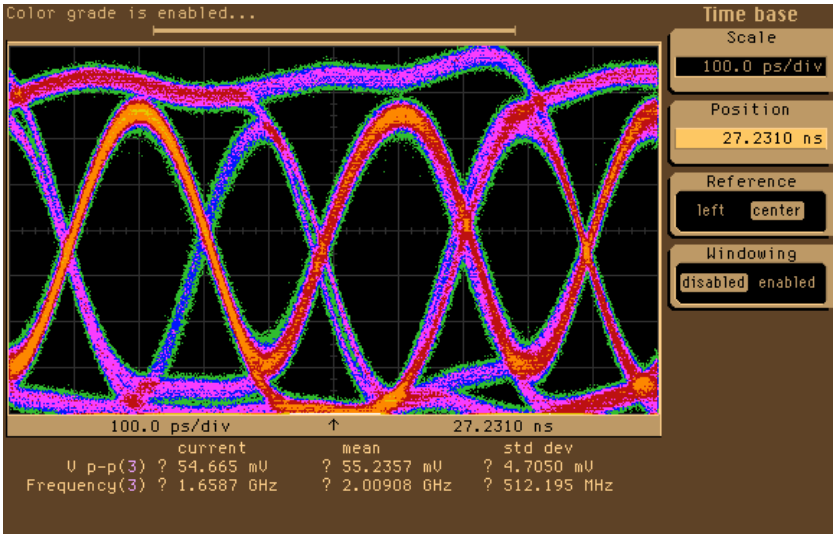

Figure 9. Test signals at 5 Gbps from the TSP-based miniature tester.

8. Conclusions

Various schemes for built-in test and built-off test are reviewed in this paper. Direct measurement techniques do not provide a viable solution for built-in test of systems with analog and RF modules because of high test resource requirements and prohibitive cost of associated test hardware. On the other hand, the inherent advantages of alternate test methodologies provide a suitable ground for implementing built-in and built-off tests for SOPs. Alternate test approaches will be used even more in the future as a combination of more intelligent load boards and on-chip test resources to address the test needs of the analog/RF modules embedded in SOPs. Built-off test is going to play a key role in multi-gigahertz digital testing as intelligent test support processors and drivers/receivers will be used to achieve high performance and reduce the capital cost of expensive high-end digital ATEs.

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