Comprehensive Catastrophic and Parametric Fault Testing Using the Alternate Test Approach

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***Abstract*— Alternate test methodology provides significant test time and equipment cost reduction for test of analog and radio frequency devices by crafting a single test stimulus and mapping the response signatures into all specifications at once. Although many previous publications reported successful implementations of alternate test, their focus has been parametric faults resulting from variations in process parameters; they do not include a systematic method to guarantee that all catastrophic faults are detected as well. In this paper, we propose a signature filtering mechanism which can be used with regular alternate test flow in order to effectively mark out catastrophic faults. The scheme makes use of a training set of parametric faults only, hence does not assume any predefined fault list. The case study on a low-noise amplifier shows that the proposed scheme can differentiate catastrophic defects with 100% coverage.**

I. Introduction

Testing state of the art analog and RF devices became a major bottleneck in high volume production further driven by the growing need for tighter quality control. The foremost problems result from the inherent complexity of the devices and the extreme sensitivity of RF signals to interference. Many different setups and test equipments are required in order to check if the device conforms to its projected performance parameters. During the high volume manufacturing, these performance parameters are measured one by one for each device and tested against defined limits called specifications. Each specification measurement requires a different test setup and a different set of test equipment. As a result, RF automatic test equipment (ATE) is put together by integrating many different benchtop components that can together accomplish a wide range of possible specification tests. Together with signal integrity, precision and repeatability concerns, the initial cost of a RF ATE becomes prohibitively expensive. Since specifications are tested one by one in a sequential manner, the operating cost also scales with the total number of specifications.

Alternate test methodology [1] provides a solution to this bottleneck by cutting down testing time and reducing the requirements on ATE. In this paper, we propose a systematic method to extend alternate test in such a way to guarantee that catastrophic and parametric faults are equally detected without any predefined fault dictionary.

A. Alternate Test Methodology

Alternate test replaces the sequential nature of many different specification tests with a single test applied to the device under test (DUT) and the response signature is mapped into all specifications at once. There are mainly two components to this flow: (i) *stimulus optimization* in which the test stimulus is carefully crafted to yield a significant correlation between the response and the specification variations, and (ii) *measurement synthesis* which constructs mapping functions from responses to specifications using supervised learning [2].

The stimulus optimization and measurement synthesis are performed on a sample set of training devices which constitute a representative set of process parameter variations present in the high volume manufacturing (HVM) environment. This way, the constructed functions can efficiently predict different specification values of a DUT given its signature response to the optimized alternate stimulus [3]. A brief review of different alternate test applications is available in [4], these examples show that alternate test provides significant test time and equipment cost reduction as well as offers built-in test solutions for analog and RF devices.

B. Analog Fault Models

The fault models for analog/RF devices and associated coverage metrics are very device dependent. Furthermore, the common open, short and bridging models only cover a small portion of possible faults. These *catastrophic faults* seriously impair the functionality of the circuit. The larger class, called *parametric faults*, usually results from process parameter variations and dictates itself as small deviations from the optimal operating point. Most parametric faults are *redundant* in the sense that the device still satisfies the datasheet specifications. Hence, modern analog test methodologies focus on specification testing rather than structural tests. Structural testing [5]–[8] usually lacks the accuracy to classify parametric failures efficiently without imposing larger yield loss. Furthermore, testing of catastrophic faults in this manner depends on a predefined fault list or a fault dictionary. Therefore, all possible catastrophic faults need to be studied extensively beforehand and the introduction of new fault modes may easily void the generated test.

Since alternate test is a specification-based methodology, its focus is on accurately detecting parametric faults. With very precise specification prediction, its ability to detect catastrophic faults is implicit because catastrophic faults generate much larger variations in response signatures. While parametric fault signatures are the focus in stimulus optimization, the catastrophic fault signatures are considered only at the HVM level with hardware samples. This way the final mappings include the range of signatures resulting from catastrophic faults. *However, this scheme still assumes that the final training set is selected in such a way to represent all members of the fault dictionary.* The alternate test literature presents no studies for cases in which the fault list is not complete or a new fault class shows up later during the manufacturing cycle.

II. Proposed Scheme

In this study, we propose a new variation of alternate test which effectively classifies catastrophic faults as well as parametric ones *without the need for a predefined fault list*. The stimulus optimization and measurement synthesis are carried out *with a training set composed of only process parameter variations* as in regular alternate test methods. In addition, we build a *signature filter* from the range of signature values within this training set. Devices with catastrophic faults have signatures significantly outside this range, hence they can easily be filtered out by this filter as faulty circuits; while regular parametric and redundant faults pass this filter and are fed into the mapping functions for specification prediction and further classification as in regular alternate test flow.

A. Signature Filter

One key step is the construction of the signature filter. An alternate signature is a set of response values processed digitally, for example: a DUT response can be sampled at a predetermined rate and digitized with a given accuracy, then the samples are converted into frequency domain using FFT, and the magnitudes of certain frequency components make up the signature. Constructing a signature filter means finding upper and lower limits for each component (ex: FFT magnitude at certain frequency bin) of the signature under process parameter variations. There are basically two methods to determine these limits: (i) deterministically using corner analyses, or (ii) probabilistically using Monte Carlo analyses. The deterministic way requires a sensitivity analysis tool which can generate precise corner data from the given netlist and process parameter variations. For high frequency RF netlists, the higher order correlations between process parameters require very complicated abstract models for efficient sensitivity analyzers. These abstract models can only be generated by a synthesis tool, which is most of the time not feasible for practical RF circuits. Hence, in this study we employed a probabilistic method, which is also inherently compatible with alternate test generation process.

The probabilistic method uses the maximum and minimum values of the signature components over the Monte Carlo set generated for measurement synthesis. In order to account for the probabilistic corners, the limits are extended by a percentage of the corresponding range. The percentage value is selected to be 25% based on the characteristics of the supervised learner MARS [9]. Furthermore, the upper limits of the responses corresponding to fundamental tones of the stimulus are extended by an additional margin. This way devices with exceptionally good operating points (designated by larger gain) are not penalized. In Section IV-B, we show a numerical example which walks the readers through filter construction.

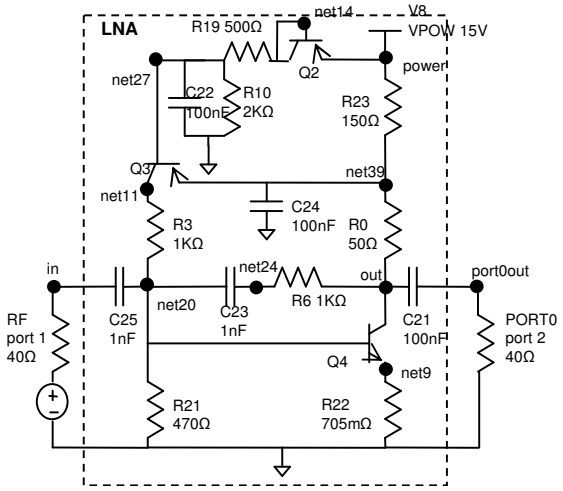

Fig. 1. 900-MHz low-noise amplifier (LNA).

III. Low-Noise Amplifier

In order to demonstrate the proposed scheme, we use a single ended 900-MHz low-noise amplifier (LNA). The LNA in Figure 1 is chosen because it is included in the Cadence RF Library [10], hence interested readers can easily duplicate and improve our experiments. Furthermore, this LNA has been the subject of different alternate test experiments in the literature [4], so the performance of the proposed scheme can be directly compared.

The 300-instance training set is generated through the Monte Carlo simulation of 6 process variables: saturation currents (I_{SN},I_{SP}) and forward gains (V_{FBN},V_{FBP}) of NPN and PNP transistors, sheet resistance (R_{sheet}) and unit capacitance (C_{base}). All variables are linearly distributed with $\pm 30\%$ variation around their nominal values. A second 100-instance validation set is also generated independently with the same distributions. Seven specifications of input-referred third order intercept point (*IIP3*), 1dB compression point (*1dBC*), noise figure (*NF*), gain (*Gain*), reverse isolation (*RevIso*), input and output standing wave ratios (*Sin*, *Sout*) are simulated and recorded for these 400 devices. The nominal, maximum and minimum values for each specification are listed in Table I together with pass/fail decision levels.

All possible opens, shorts and bridges are considered for catastrophic faults. Over 200 possible variations morph to

TABLE I

SPECIFICATION STATISTICS OVER VALIDATION SET

Spec	Unit	Nom	Max	Min	P/F	UHL	LHL
IIP3	dBm	1.84	7.65	-1.1	> -0.8	10	-4
1dBC	dBm	-10.7	-4.8	-13.9	> -13.5	0	-18
NF	dB	4.1	5.3	3.74	< 6	8	0
Gain	dB	14.5	15.1	11.6	> 12.4	15	8
RevIso	dB	31.6	32.4	30.9	> 20	35	15
Sin	/	2.2	2.8	1.8	< 8	10	0
Sout	/	1.09	2.1	1.06	< 8	10	0

P/F: pass fail boundary, UHL/LHL: upper/lower hard limits

TABLE II

MAXIMUM AND RMS SPECIFICATION PREDICTION ERRORS

Spec	Unit	Rms	Max
IIP3	dB	0.05	0.20
1dBC	dB	0.09	0.30
NF	dB	0.01	0.03
Gain	dB	0.02	0.13
RevIso	dB	0.01	0.06
Sin	/	0.01	0.02
Sout	/	0.01	0.04

for parametric faults only with regular alternate test

48 distinct faults. All faults are manually inserted into the netlist and devices are simulated for seven specifications under test. Due to the nature of catastrophic faults, some specifications may have extreme values. For example, for an instance with no gain, the 1dB compression point hypothetically goes to infinity. In order to better handle these extreme values, each specification value is limited by an upper and a lower hardbound as listed in Table I.

In order to cover a variety of catastrophic faults, we have simulated additional instances by replacing each resistor and capacitor with other ones at 1000-times, 10-times, 1.5-times, $1/1000^{th}$, $1/10^{th}$ and half of their original values. This way we introduced 78 extra fault modes, 6 for each capacitor and resistor value. Also, we have simulated 5 other fault modes which represent ground bounces and resistive power paths.

All together it comes to 100 candidates for *parametric faults* (validation set) and 131 candidates for *catastrophic fault*s. 57 out of 131 are actually *redundant faults* meaning that all of their specifications are within the pass limits listed in Table I. 80 out of 100 instances in the validation set are also within pass limits.

IV. ALTERNATE TEST IMPLEMENTATION

A. Alternate Test without Signature Filter

First we present the results for a regular alternate test scheme using the data set and circuit discussed in Section III. The optimized stimulus has two tones each with -8dBm power at 900MHz and 920MHz. The responses are sampled, digitized and converted to frequency domain by a 1024-point FFT operation. The amplitudes of 13 frequency components from 780MHz to 1020MHz separated by 20MHz constitute the signature. The mapping functions are generated with the 300-instance training set. The key point here is that training set only includes instances with parametric faults.

Figure 2 shows the ISO graphs of six specifications (*Sout* is similar to *Sin*) for the 100-instance validation set, where x-axis marks the actual specification value obtained through simulation and y-axis marks those predicted by alternate test. The 45° line shows the ideal prediction, while Table II lists the maximum and rms errors for each specification. All instances are correctly classified giving 100% fault coverage and 0% yield loss.

However, when we feed in the signatures from 131 catastrophic fault candidates, 13 instances are misclassified, 3 of which are very critical false positives meaning that they actually fail at least one specification limit yet their predicted values show otherwise. *This example shows that when alternate mapping functions are not trained with a representative set including possible catastrophic faults, they are doomed to fail as any other supervised learner. On the other hand, since alternate HVM mappings are based on a training set of hardware instances including catastrophic faults, this is still not a set back for regular alternate test methodologies.*

B. Signature Filter with Alternate Test

Next we repeat the experiment in Section IV-A with the proposed methodology. The signature filter is constructed as follows: (i) determine maximum and minimum values for each signature component over the 300-instance training set (dotted lines in Figure 3); (ii) enlarge the signature limits by $\pm 25\%$ of the range (solid lines in Figure 3); (iii) add an additional 3dB margin to the maximum limits for 900MHz and 920MHz fundamental responses. Table III lists the maximum/minimum values and filter upper/lower bounds for each signature component.

All the signatures in the 100-instance parametric validation set pass the signature filter, hence the ISO graphs are exact copies of Figure 2 and prediction errors equals the ones listed in Table II. The real difference comes from 131-instance catastrophic fault candidate set. *The signature filter identifies all 74 of catastrophic faults, hence gives 100% fault coverage.* 3 out of 57 redundant faults are also eliminated by the signature filter. The rest of the redundant faults are passed into the alternate mappings for further classification and only 4 are false negatives with no false positives. *Overall, the alternate mappings with the signature filter scores 100% fault coverage on the 131-element catastrophic fault candidate set.* Note that these results are obtained by training on the parametric fault set only, and without any fault list assumptions for catastrophic faults.

C. Signature Filter with Extra Training

Although the results in Section IV-B are promising, the prediction accuracy for the redundant faults is still low,

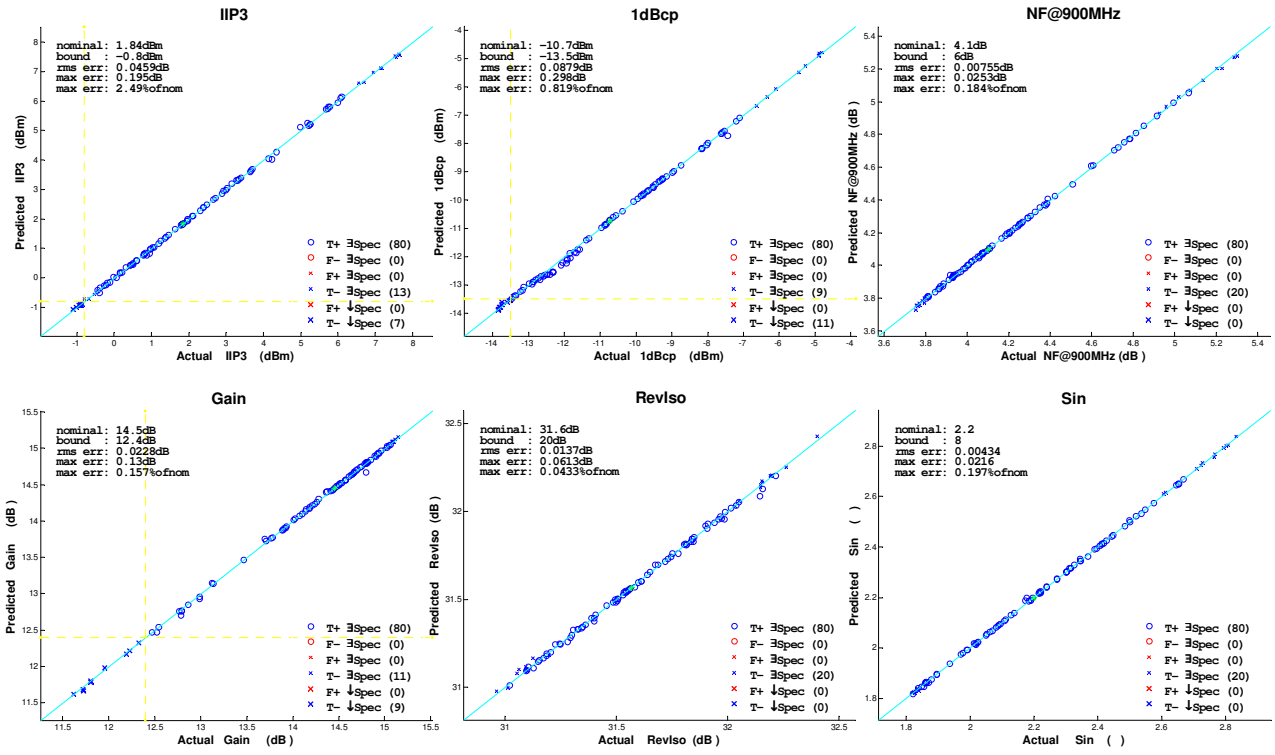

Fig. 2. ISO graphs for regular alternate tests over the 100-instance validation set with process parameter variations. Specification predictions in y-axis for IIP3, 1dB compression point (1dBcp), noise figure (NF), gain, reverse isolation (RevIso) and input standing wave ratio (Sin); 45° line shows the ideal mapping; dotted vertical and horizontal lines mark pass/fail boundaries; correctly classified passing parts are marked with blue 'o's while correctly classified failing marks are in blue 'x's; no misclassification.

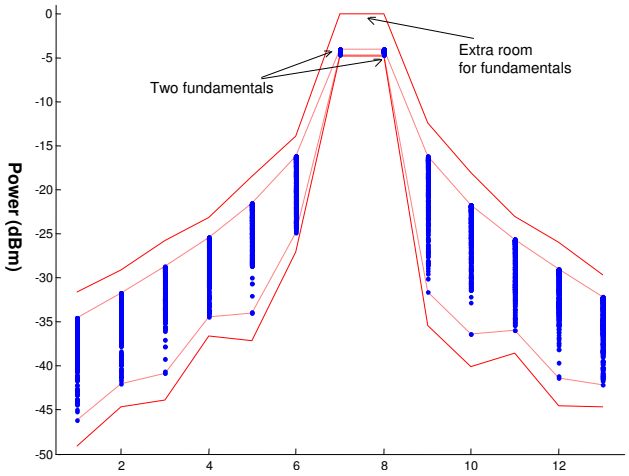

Fig. 3. Signature filter; dotted lines show the maximum and minimum signature components while solid lines show signature filter upper and lower bounds after added margins.

TABLE III
SIGNATURE FILTER UPPER AND LOWER BOUNDS

Frequency	max	min	lower	upper
MHz	dBm	dBm	dBm	dBm
780	-34.56	-46.18	-49.08	-31.66
800	-31.67	-42.07	-44.67	-29.06
820	-28.73	-40.82	-43.85	-25.71
840	-25.40	-34.39	-36.64	-23.16
860	-21.55	-34.00	-37.12	-18.43
880	-16.15	-24.86	-27.04	-13.97
900	-4.032	-4.65	-4.81	-0.207
920	-4.060	-4.67	-4.82	-0.217
940	-16.23	-31.57	-35.40	-12.39
960	-21.69	-36.39	-40.06	-18.01
980	-25.60	-35.99	-38.58	-23.00
1000	-29.05	-41.43	-44.52	-25.95
1020	-32.19	-42.18	-44.68	-29.69

because the training set does not include any examples of this kind. In this part, we present the results for a more realistic experiment, where the training set is expanded by a list of redundant faults. For this experiment, we generate an additional 200-instance training set with single variations in the range of 10-times to $1/10^{th}$ of the component value. These variations are added on top of the $\pm 30\%$ linearly distributed process parameter variations. We use the exact same signature filter in Section IV-B, so that signature filter limits are only determined by the process parameter variations.

The MARS mappings are trained by the original 300-instance set plus the new 200-instance set. Figure 4 shows

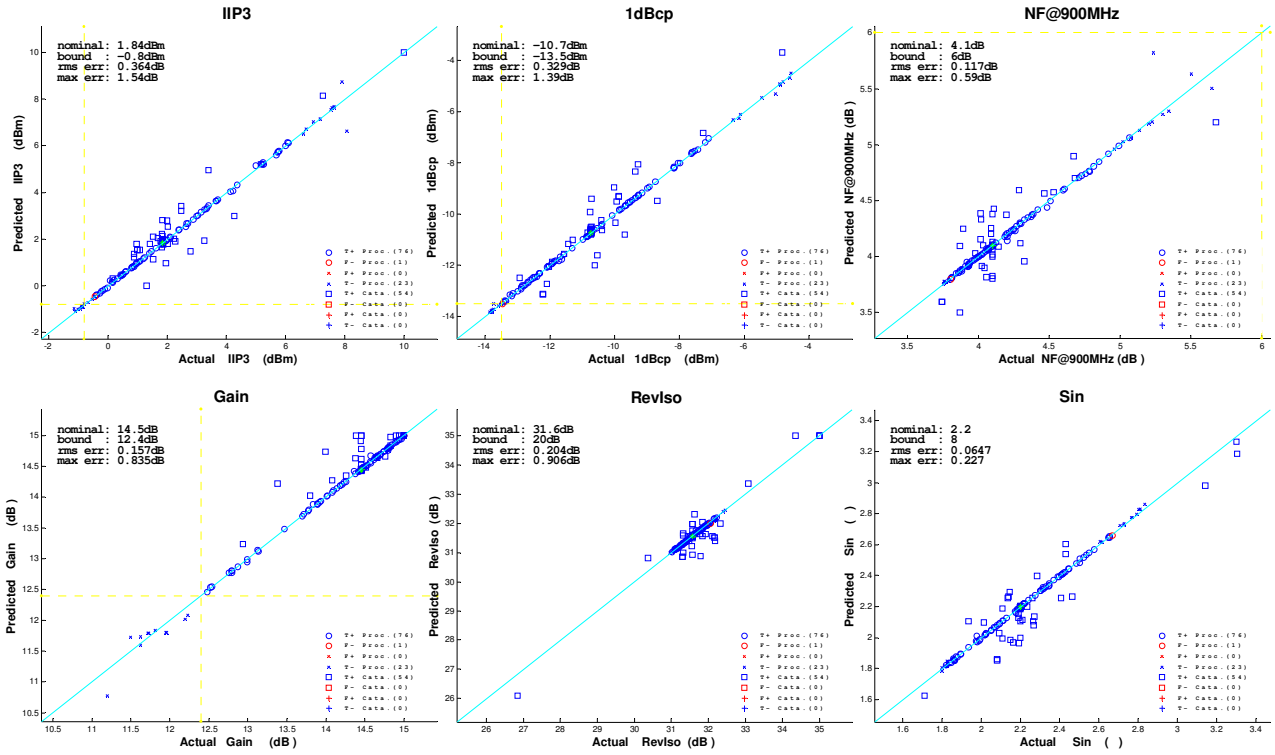

Fig. 4. ISO graphs for proposed alternate tests with signature filter over the 100-instance validation set and redundant faults. Specification predictions in y-axis for IIP3, 1dB compression point (1dBcp), noise figure (NF), gain, reverse isolation (RevIso) and input standing wave ratio (Sin); 'o's and 'x's represent the instances in the validation set while redundant faults are marked with squares; the only false negative is from the validation set and marked with a red 'o'.

TABLE IV

SPECIFICATION MAXIMUM AND RMS PREDICTION ERRORS

		Parametric		Catastrophic		Both	
Spec	**Unit**	**rms**	**max**	**rms**	**max**	**rms**	**max**
IIP3	dB	0.02	1.43	0.57	1.54	0.36	1.54
1dBC	dB	0.05	0.27	0.55	1.39	0.33	1.39
NF	dB	0.06	0.59	0.18	0.47	0.12	0.59
Gain	dB	0.06	0.42	0.25	0.83	0.16	0.83
RevIso	dB	0.02	0.09	0.34	0.91	0.20	0.91
Sin	/	0.01	0.04	0.11	0.23	0.07	0.23
Sout	/	0.01	0.06	0.07	0.20	0.04	0.20

for parametric and catastrophic faults after signature filter

the ISO graphs for specification predictions. The "o"s and "x"s represent the passing and failing components in the 100-instance validation set, whereas squares represent the predictions for redundant faults in the 131-instance catastrophic fault candidate set. Table IV lists the rms and maximum prediction errors for parametric fault set, catastrophic fault set (redundant faults) and both together. There is 1 false negative in the validation set classification. Note that all 74 catastrophic faults are correctly identified by the signature filter, where only 3 of the redundant faults are misclassified. *The rest of 57 redundant faults are correctly classified by the mappings, yielding a total of 100% fault coverage over 231 instances (validation set + catastrophic fault candidate set).*

V. CONCLUSIONS

The proposed signature filter correctly classifies all catastrophic faults without the need for a predefined fault library. However, yield loss and prediction error are high when there are no redundant fault examples in the training set. Prediction accuracy can be significantly improved by adding a second training set which assumes a larger and isolated component variation. The methodology described provides a simple extension to alternate test methodology for HVM environments with new fault classes showing up later during the manufacturing cycle.

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REFERENCES

[1] P. Variyam, S. Cherubal, and A. Chatterjee, "Prediction of analog performance parameters using fast transient testing," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 21, no. 3, pp. 349–361, 2002.

[2] T. Hastie, R. Tibshirani, and J. H. Friedman, *The Elements of Statistical Learning: Data Mining, Inference, and Prediction*. Springer-Verlag, New York, NY: Springer Series in Statistics, 2001.

[3] R. Voorakaranam, S. Cherubal, and A. Chatterjee, "A signature test framework for rapid production testing of RF circuits," in *Proc. Design, Automation and Test in Europe*, Paris, France, Mar. 2002, pp. 186–191.

[4] S. S. Akbay, J. L. Torres, J. M. Rumer, A. Chatterjee, and J. Amtsfield, "Alternate test of RF front ends with IP constraints: Frequency domain test generation and validation," in *Proc. International Test Conference*, 2006.

[5] L. Milor and V. Visvanathan, "Detection of catastrophic faults in analog integrated circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 8, no. 2, pp. 114–130, Feb. 1989.

[6] A. McKeon and A. Wakeling, "Fault diagnosis in analogue circuits using AI techniques," in *Proc. International Test Conference*, Washington, DC, USA, Aug. 1989, pp. 118–123.

[7] N. B. Hamida and B. Kaminska, "Multiple fault analog circuit testing by sensitivity analysis," *Journal of Electronic Testing: Theory and Applications*, vol. 4, pp. 331–343, 1993.

[8] G. Devarayanadurg and M. Soma, "Analytical fault modeling and static test generation for analog ICs," in *Proc. International Conference on Computer-Aided Design*, San Jose, CA, USA, Nov. 1994, pp. 44–47.

[9] J. H. Friedman, "Multivariate adaptive regression splines," *The Annals of Statistics*, vol. 19, no. 1, pp. 1–141, Apr. 1991.

[10] *Affirma RF Simulator (SpectreRF) User Guide*, Section 6, pp. 4, Cadence Design Systems Inc., 1999.