A CMOS Visible Image Sensor Array Using Current Mirroring Integration Readout Circuitry

S.S. Akbay[2], A. Bircan[2], and T. Akin[1,2]
[1]Middle East Technical University, Dept. of Electrical and Electronics Eng., Ankara, Turkey
[2] TUBITAK-ODTU-BILTEN, Middle East Technical University, 06531 Ankara, Turkey
e-mail: tayfun-akin@metu.edu.tr http://www.eee.metu.edu.tr/~tayfuna

Summary. *This paper reports the development of a CMOS visible sensor array using a high performance readout circuit called Current Mirroring Integration (CMI). The sensor element is a photodiode implemented using n-well and p^+-active layers available in any CMOS process. The current generated by optical excitation is mirrored and integrated in an off-pixel capacitor using the CMI readout circuit, which provides high injection efficiency, low input impedance, almost-zero and stable detector bias, and a high dynamic range. A 16x16 test array is fabricated using a 0.8µm CMOS process. Each detector pixel in the array occupies a 50µm x 50µm area with a fill factor of 60%. Operation of the fabricated test array is verified, and the output dynamic range is measured as 0.5V to 4.8V.*

Keywords: visible image sensors, readout electronics, CMOS sensors

Introduction

Imaging systems have widespread applications in cameras, military systems, medical examinations, and astronomical observations. Lately, most widely used CCD type imagers are challenged by CMOS imagers that have advantages like low cost, low power consumption, and integration with on-chip image enhancement and digital processing capability [1]. It is expected that performance of the CMOS imagers will be even better than CCD imagers [2].

One of the most important factors in the performance of CMOS imagers is the readout circuit. A high performance readout structure should provide a stable near-zero detector bias to reduce dark current and detector noise, should have a small input resistance to provide high injection efficiency, and should utilize a large dynamic range to increase the maximum charge storage capacity with a small pixel area and high resolution for the focal plane array. Various readout circuits have been used in CMOS imagers, including simple photodiode type passive pixels, photodiode type active pixels, photogate type active pixels, logarithmic type pixels, floating gate pixels, and shared buffer direct injection readouts [1]. However, these readout circuits have various drawbacks, and none of them completely satisfies the high performance measures listed.

Recently, we have developed a new, high performance readout circuit called Current Mirroring Integration (CMI) for infrared focal plane arrays [3]. This paper reports the use of CMI readout circuitry in a CMOS imager to achieve stable and near zero detector bias, high injection efficiency, and high dynamic range.

Pixel Structure and Operation

Figure 1 shows the structure of the CMOS visible image sensor. Photodetectors in each pixel are implemented with a p-n junction diode using n-well and p^+-active diffusion layers that are available in any CMOS process. The detector diode in each pixel is reverse biased, and when incoming photons are absorbed, a photocurrent proportional to the intensity of light flows through the diode. This current is converted to an output voltage value using the CMI readout circuit.

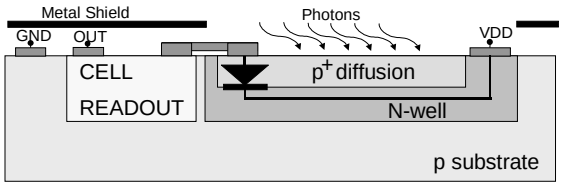

Fig. 1: The structure of CMOS visible image sensor. p-n junction diode is implemented with p+ diffusion and n-well.

Figure 2 shows the structure of the Current Mirroring Integration (CMI) readout circuit. The induced current on the reversed biased detector diode is copied through a high-swing cascoded nMOS current mirror and is fed to the pMOS current mirror. These two current mirror structures result in an almost-zero detector bias, reducing the dark current and improving detector's noise performance. This fact can be demonstrated by analytical calculations. Figure 3 shows a simplified structure of the CMI circuit used in analytical calculations. Considering that transistors operate under the weak inversion condition, the detector bias can be calculated with the following equation:

$$V_{DET} = \frac{K_N}{K_P} \times \Delta V_{TN} + \Delta V_{TP} \qquad \text{(Eq. 1)}$$

where K_N and K_P are the geometry constants of the nMOS and pMOS transistors, and ΔV_{TN} and ΔV_{TP} are the threshold voltage mismatches [4]. If the transistor geometries are equal, then the detector reverse bias voltage becomes only a few milivolts for typical CMOS process variations. For example, a 1% mismatch on threshold voltages of 0.75V results in a 15mV voltage bias on the detector in a 0.8μm CMOS process.

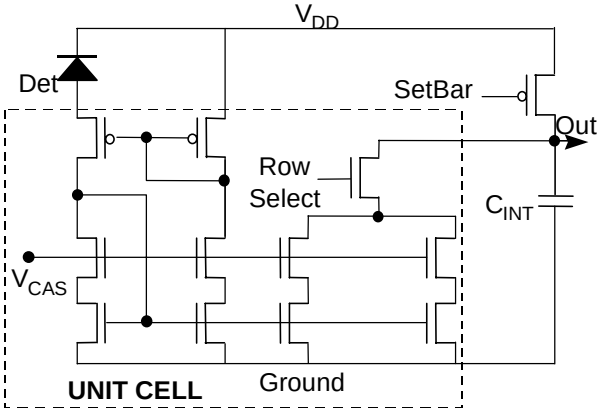

Fig. 2: Schematic view of the Current Mirroring Integration (CMI) readout structure. Note that integration capacitance resides outside the unit cell.

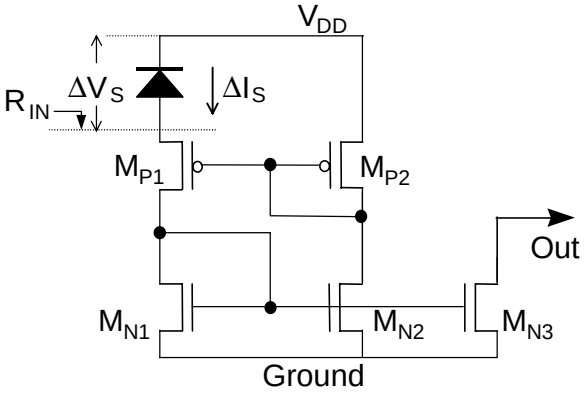

Fig. 3: Schematic view of the simplified Current Mirroring Integration structure used in the analytical calculations.

Another advantage of the current mirror feedback structure is that it provides a very low input resistance, resulting in almost unity injection efficiency. This input impedance can analytically be calculated by determining the change in voltage, ΔV_S, due to the change in detector current, ΔI_S [4]. By defining γ as:

$$\gamma = \frac{g_{mN2}}{g_{mN1}} \times \frac{g_{mP1}}{g_{mP2}} \qquad \text{(Eq. 2)}$$

the relation:

$$g_{mP1} = \frac{\Delta I_S}{\Delta V_{GP} - \Delta V_S} \qquad \text{(Eq. 3)}$$

yields the following impedance:

$$R_{in} = \frac{\Delta V_S}{-\Delta I_S} = \frac{1-\gamma}{g_{mP1}} \qquad \text{(Eq. 4)}$$

where g_{mN1}, g_{mN2}, g_{mP1}, and g_{mP2} represent the transconductances of the N1, N2, P1, and P2 transistors, respectively.

By using proper layout techniques, γ can be made quite close to unity, hence yielding near-zero input impedance and unity injection efficiency. For a γ of 99.9% and a typical g_{mP1} of 2μA/V, R_{IN} can be reduced to a value as low as 500Ω. The main deficiency in obtaining unity injection efficiency comes from the difference in g_m values due to process variations and short-channel effects. By using the high-swing cascode current mirror in Figure 2 instead of the single current mirror mentioned in the analytical calculations, high current mirroring performance and better matching in g_m values can be achieved. These calculations show that the CMI circuit provides an almost zero and stable detector bias and has a very low input impedance, resulting in almost unity injection efficiency.

Array Design and Implementation

A 16x16 imager array is designed using a 0.8μm CMOS technology to demonstrate the use of CMI readout structure in visible arrays. One of the advantages of the CMI readout circuit is that it is possible to place the integration capacitance outside of the unit cell, as shown in Figure 2. This helps to reduce the unit cell area and at the same time to obtain a higher charge storage capacity. The current from the CMI unit cell is transferred to the external integration capacitor through a row select transistor. The rows are selected one after another by the scanning registers while all the pixels of a column share the same integration capacitor one at a time. It is also possible to include a number of capacitor sets with different capacitance values and select one set according to the specifications of the scene. This feature provides a flexible tradeoff between average light intensity and resolution of the light intensity. For example, a large capacitor set can be used with a quite bright scene, while a smaller capacitor set can be used with a less bright scene, obtaining the same sensitivity to dynamic range ratio in both cases.

Figure 4 shows the overall data path for the focal plane array. Each capacitor in the array is followed by a buffer-connected operational transconductance amplifier with almost rail-to-rail operation; the rail-to-rail operation is necessary for high dynamic range. Outputs of all columns are multiplexed by the column select circuitry and connected to a correlated double sampling (CDS) device to reduce noise. During reset of the selected row, a clamping signal is generated, and the clamping capacitor is discharged to the reset noise of the row parasitics. This noise is subtracted from the multiplexed signal to suppress

both the switching noise and the offset voltages induced by the buffers.

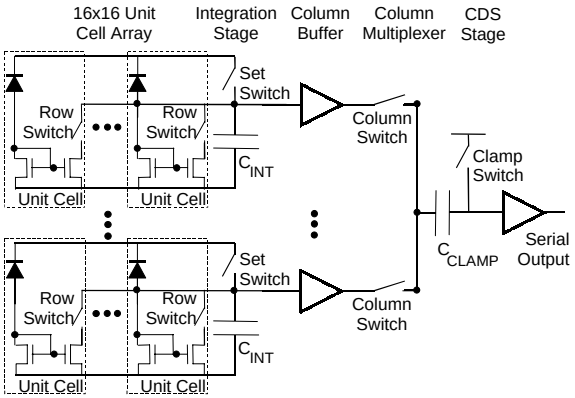

Fig. 4: Overall datapath for the focal plane array. The integration capacitor voltage is buffered and multiplexed by the column select switches. The multiplexed data is processed by the correlated double sampling (CDS) circuit and a single serial output is generated.

Figure 5 shows the timing diagram for this focal plane array scanning circuitry. All digital control signals for multiplexer and correlated double sampling circuitry are generated on-chip by robust scanning electronics.

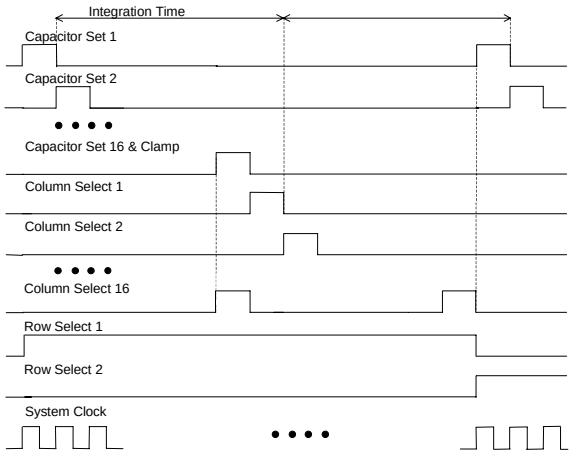

Fig. 5: The timing diagram for the focal plane array scanning circuitry. A full frame contains 16 non-overlapping row select signals, hence it is 32 times the integration time. All signals are generated by a single input, the system clock.

Figure 6 shows the simulation results for the unit pixel for different imager currents ranging from 10nA up to 60nA with a 2pF integration capacitor. The simulations show that the CMI structure employs %99 linearity and a rail-to-rail dynamic range at the integration capacitor. It is important to have a buffer with high dynamic range and linear operation to transfer this linear signal on the integration capacitor to the output without degrading its linearity and limiting its dynamic range.

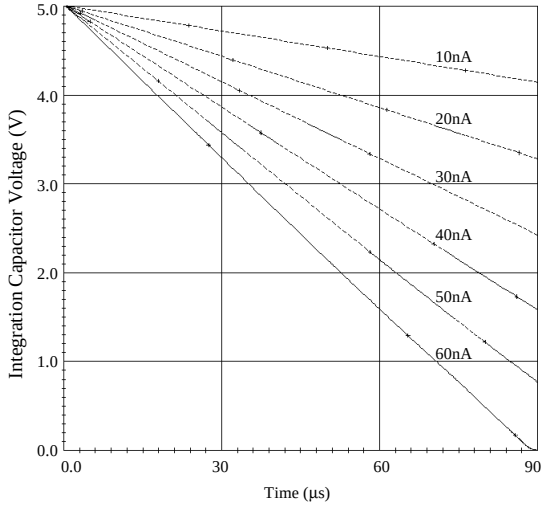

Fig. 6: Simulation results of the CMI circuit for detector currents of 10nA to 60nA when the integration capacitor is 2pF. The CMI structure exhibits a rail-to-rail operation with %99 linearity.

A layout of the 16x16 image sensor test array was prepared using a 0.8µm CMOS process. Figure 7 shows the 50µm x 50µm unit pixel layout, which contains 9 transistors and the photodiode with a fill factor of %60. Figure 8 shows the layout of the 16x16 test array, which occupies an area of 1200µm x 1700µm.

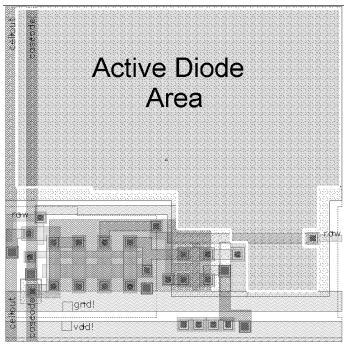

Fig. 7: Layout of the detector pixel with a 50µm x 50µm area in a 0.8µm CMOS process. The unit cell contains only 9 transistors and a photodiode with a fill factor of 60%.

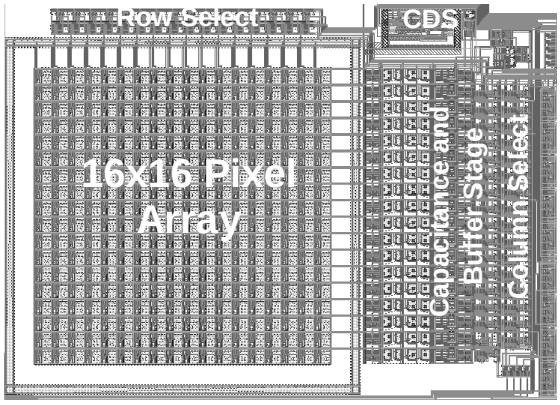

Fig. 8: The layout of the 16x16 test array which occupies an area of 1200µm x 1700µm.

Fabrication and Test Results

The test array was fabricated in a 0.8μm double-poly double-metal CMOS process. Figure 9 shows a close up microphotograph of the fabricated 16x16 test array, showing few pixels. The bottom left part of the unit cells are the CMI readout transistors shielded by the second metal layer.

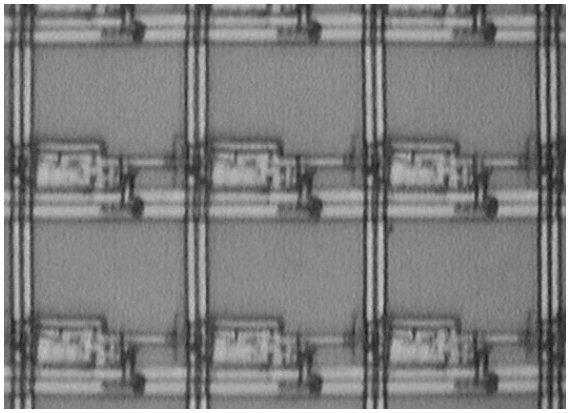

Fig. 9: The close up microphotograph of the fabricated 16x16 test array showing few pixels. The bottom left part of the unit cells are the CMI readout transistors shielded by the second metal layer.

A number of tests were performed to verify the operation of the 16x16 imager array. Table 1 summarizes the overall measurement results. The tests show that the circuit operates as designed. Figure 10 shows the output of a single column for different light intensities. The trace at the bottom has been saturated and displays an almost rail-to-rail dynamic range of 4.8V down to 0.5V with linear operation. The integration time for these samples is 5ms, corresponding to only 6 frames/s operation; however, measurements show that the array can run up to 300 frames/s with an integration time of 100 μs and has a total power dissipation of 4mW. The circuit can be modified to provide a higher frame rate for a larger array size.

Table 1: The measurement results and operation conditions for the 16x16 CMOS visible imager.

Parameter	Results
Technology	0.8 μm CMOS
Pixel Pitch	50 μm x 50 μm
Fill Factor	60%
Maximum Output Swing	4.8V to 0.5V
Maximum Readout Speed	300 frames/s
Linearity	99%
Integration Time	100 μs
Typical Integration Cap.	2 pF
Maximum Input Current	100 nA
Power Supply	0-5 Volts
Power Dissipation	4mW
Operating Temperature	25°C

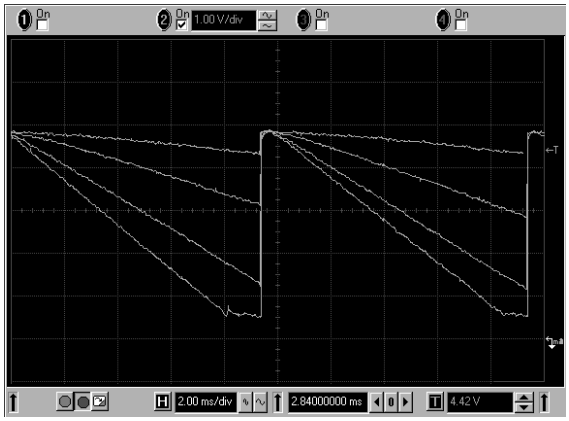

Fig. 10: The output of a single column of the focal plane array for different light intensities, where four of the stored waveforms are displayed together for demonstration. The saturated trace at the bottom displays a linear response with an almost rail-to-rail dynamic range of 4.8V to 0.5V at the buffer output.

Conclusion

A high performance CMOS visible image sensor array has been designed and fabricated. The imager uses Current Mirroring Integration (CMI) readout circuit to achieve a stable near-zero detector bias, high injection efficiency, and a large linear dynamic range. The fabricated 16x16 test array shows that this structure is suitable for large and low power focal plane array imaging applications.

Acknowledgements

Authors would like to thank Mr. Haluk Kulah for his idea of the CMI structure and use of it in visible imagers. This research is a part of the TU-MICROSYSTEMS project, which is sponsored by NATO's Scientific Affairs Division in the framework of the Science for Stability Programme. Authors also would like to thank ASELSAN Inc. for their encouragement and support of this work.

References

[1] E. R. Fossum, "CMOS image sensors: Electronic camera-on-a-chip," *IEEE Trans. on Electron Devices*, vol. 44, no. 10, (1997) 1689-1698.

[2] L. J. Kozlowski, D.Standley, J.Luo, A.Tomasini, A.Gallagher, R.Mann, B.C.Hsieh, T.Liu, and W.E.Kleihans, "Theoretical basis and experimental confirmation: why a CMOS imager is superior to a CCD," *Infrared Tech. and App. XXV, Proc. SPIE*, vol. 3698, pp. 388-396, April 1999.

[3] H.Kulah and T.Akin, "A CMOS current mirroring integration readout structure for infrared focal plane arrays," *Proc. 24th European Solid-State Circuits Conf.*, pp. 468-471, The Hague, September 1998.

[4] N. Yoon, H. C. Lee, H.Shin, and C.K. Kim, "A New Unit Cell of Current Mirroring Direct Injection Circuit for Focal Plane Arrays," *Infrared Technology and Applications XXII, Proc. SPIE*, vol. 3061, pp. 178-181, April 1997.