Built-In Test of RF Components Using Mapped Feature Extraction Sensors

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Abstract -- *At low frequencies, alternate testing is based on sampling the test response using an A/D converter and analyzing the digitized response in the external tester. In order to use alternate test at frequencies in the multi-GHz range, where the above is not possible, the test waveforms need to be very simple and the evaluation of the test response needs to be handled by on-chip analog test response "feature extractors". In this work, specialized functions of the output response from an alternate test are computed using built-in feature extraction sensors, which measure a complex function of the response waveform and output a DC signature. Different sensor structures are evaluated based on their performance in the presence of environmental effects and process shifts It is seen that very simple sensing circuitry can predict high quality alternate test for RF components..*

1. Introduction and Objectives

The challenge of keeping up with the ever-increasing operating frequency of the device under test (DUT) has initiated a paradigm shift in high speed analog testing favoring alternative approaches such as built in test (BIT) where the test functionality is brought to the closest possible proximity of the DUT, that is, into the chip/package. This scheme can make use of a low cost external tester connected through a low bandwidth link in order to perform demanding response evaluations, as well as make use of the analog to digital converters (ADC) and digital signal processors (DSP) available on the chip/package to facilitate testing. In Systems-on-Packages (SOPs), test problems due to signal integrity, I/O bandwidth, and limited controllability and observability make BIT a necessity. Although recent research on analog BIT has demonstrated hardware solutions for single specifications, the paradigm shift calls for a rather general approach where a single methodology can be applied across different devices and multiple specifications can be verified through a single test hardware unit minimizing area overhead. In this paper, we propose an extension of the alternate test methodology that is suitable for BIT of multi-GHz analog and radio frequency (RF) components packaged in an integrated environment. There are two key contributions of this work:

- We propose *simple sensor structures* instead of conventional rms or peak detectors. The conventional detectors are very accurate but complex in structure hence occupy large area, comes with significant parasitics and need elaborate calibration schemes to satisfy the region of operation. In contrast, *our sensors are simple yet still able to yield accurate specification prediction with alternate test.*
- The proposed methodology can compensate these simple on-chip sensors for *environmental effects such as due to temperature as well as process variations without additional compensation circuitry.*

The paper is structured as follows: the fundamentals are handled in Section 2, where we review the alternate test methodology. Section 3 discusses associated test challenges for multi-GHz alternate test and summarize the solutions proposed. Section 4 elaborates on one such solution, namely DC level feature extractors. Section 5 gives an implementation of the proposed *implicit feature extraction*, called as *differential-topology sensors*, as well as a technique to compensate these on-chip sensors for thermal variations. Section 6 describes another class of implicit feature extractors, *recursive sensors*, which are capable of tracking large process shifts.

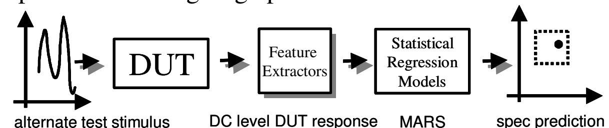

Figure 1: Alternate test methodology.

2. Alternate Test Basics

In s*pecification-based alternate tests*, the data sheet specifications of a DUT are predicted by analyzing its response to a specific input pattern, which is carefully crafted to yield a significant correlation between the response and the specification variations. The DUT response can be considered as a signature of the effects of process variations specific to that DUT instance. The variations in any process variable in the circuit parameter space P, affect both the circuit specification space S, and the response measurement space M. Two different non-linear mappings define these relationships: $f_{ps}: P \rightarrow S$ and $f_{pm}: P \rightarrow M$. Nonlinear statistical multivariate regression analysis allows one to construct a function $f_{ms}: M \rightarrow S$ such that for a given set of measurements, the mapping generates predictions for the values of the specifications-under-test [1].

Figure 1 summarizes the specification-based alternate test methodology: an alternate test stimulus is applied to DUT and the DUT output is fed to the feature extractors; in the next step, the collected data from feature extractors

is applied to statistical regression models, which predict specifications-under-test.

Section 4 in [2] covers an extensive bibliography of recent research on analog BIT. These implementations propose customized hardware solutions valid for single specifications-under-test. This introduces significant area overhead since multiple specification measurements require different kind of resources. Furthermore, most of the BIT schemes only provide pass/fail decisions in the presence of catastrophic faults. There are only a few approaches, such as [3], which can generate quantitative measures for selected number of specifications; however, the measurement-to-specification mappings have to be hand-crafted specifically to the characteristics of the DUT. *On the other hand, specification-based alternate test provides a general methodology independent of the DUT or the target specifications.* In this sense, it is a complete tool which can be applied across different devices, and multiple specifications can be verified through a single data acquisition, thereby minimizing area overhead.

3. Prior Work: Alternate Test at Multi-GHz

At low frequencies, alternate testing of analog modules is based on sampling the test response using an ADC and analyzing the digitized response in the external tester. The sampling of the signature is a critical part of the alternate test procedure and such that the speed and accuracy of sampling mostly defines the accuracy of predictions. For RF components operating in the gigahertz range, this requirement causes a problem, since the Nyquist sample rate of such signals and their harmonics may far exceed the capabilities of ADCs already present on-chip. In order to use alternate test at frequencies in the multi-GHz range with analog and RF components, the test waveforms need to be very simple and the evaluation of the test response needs to be handled in a way that avoids high speed A/D conversion. Previous work has demonstrated three different solutions: the first scheme [4] implements upconversion and downconversion of a baseband signature; the second [5] makes use of an optimization algorithm to find the lowest frequency stimulus that can satisfy predefined prediction accuracy; and the third [6] implements a digital-BIST compatible approach based on reliable subsampling. The reader may refer to [7] for a detailed comparison of these methodologies. Recently, Bhattacharya and Chatterjee in [8] proposed a detector-based implementation, which makes use of hardware-based test response feature-extractors to produce a DC signature of the alternate response. Although this experiment demonstrates the potential of DC level sensors used together with alternate tests for BIT, explicit features, such as peak or rms, require the use of complex circuitry for measuring the corresponding peak and rms values.

4. DC Level Feature Extractors

DC level feature extraction has been used in measurement setups in the past to measure properties of electrical signals such as bias current/voltage, peak, root-mean-square (rms), zero-crossing and tuned spectral components using *explicit feature extraction circuitry* (*or feature detectors*). The circuitry associated with such detectors is generally complex (an rms detector generates a DC voltage proportional to the rms value of the signal). In addition, the DC voltage generated is almost always an approximation to the signal feature measured. This is generally due to the nonlinearities present in the devices used to design the detector. The use of bipolar devices results in better characteristics and is preferred over the use of field effect transistors. However, even bipolar based applications require post-production calibration for accuracy. To make matters worse, on-chip feature detectors suffer from process variation and thermal effects that impact the performance of on-chip circuitry that the detectors are designed to monitor. In RF circuits, it is possible for the detector size to approach the RF DUT size, shifting the test focus from the DUT to the detector.

To alleviate the above problems with conventional DC level feature detectors (such as rms/peak detectors) we propose a new class of *function-mapped (Fmap) sensors* (detectors). These *Fmap*-sensors generate *predetermined functions* of an electrical signal as opposed to specific rms/peak values. This has several benefits: (a) the sensor designer can choose a *simple sensor design* and use the resulting function of the input signal the sensor generates to perform test (as opposed to designing a complex *exact* rms detector) and (b) by *combining the use of these Fmap-sensors with the alternate test approach*, the test specifications of the DUT can be predicted with an accuracy that is only possible with elaborate post-production calibration of traditional sensors and additional complex circuitry to take care of process variations. This presents a new sensor paradigm for use with alternate test methodology. Since the measurements in alternate tests are different from those made in classical specification based tests, the built-in sensors used for measuring classical figures of merits such as peaks, root-mean-square values, zero-crossings, etc can be replaced with *Fmap-sensors* that measure figures that are more accessible but harder to relate to the specification value. *The mapping process in alternate test will build a good enough prediction as long as the changes in the measured figure are correlated to the specifications under test.*

In order to validate the idea, we have implemented two different classes of Fmap-sensors and demonstrated their auto-calibration abilities in the presence of environmental variations and large process shifts.

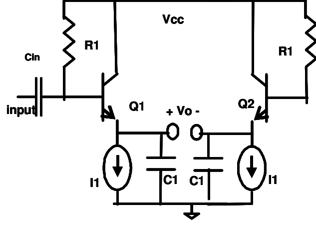

Figure 2: BJT-based differential-topology sensor.

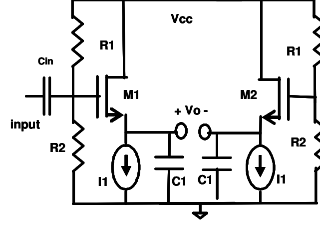

Figure 3: FET-based differential-topology sensor.

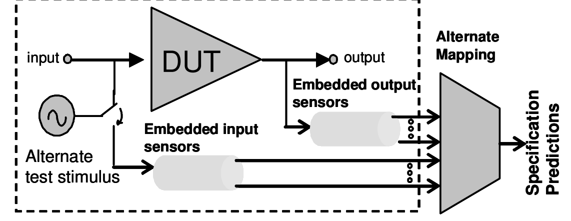

Figure 4: BIT setup with differential-topology sensors.

5. Differential-Topology Sensors

The peak detector implementation in Figure 2 represents a high-end example for common explicit feature extractors; its differential nature helps protect against process and environmental variables, and it provides a more linear mapping when compared to FET/diode-based peak detectors, yet keeping a simple structure with low transistor count [9]. However, even this implementation needs calibration for extending its limited region of operation. Moreover, its output is proportional to the peak of the signal provided that the signal is a sinusoidal. For distorted waveforms its accuracy fades dramatically destroying the one-to-one mapping. In [10], a hardware modification is proposed to implement a more linear transfer function, keeping its relative error in the 8% range. On the other hand, this modification makes the implementation more complicated, and adds significant area overhead. Our experiments suggest that in the presence of regular process and temperature variations, the relative error for the original circuit is 42% excluding the problematic transition region, and the error goes up to 63% after the hardware modifications proposed in [10], making it unsuitable for built-in test environments.

Following the derivation in [7], the output of this sensor can be represented as:

$$V_o = V_t \cdot \ln\left(e^{\frac{x(t)}{V_t}} \Big|_{dc} \right) \quad (1)$$

The derivations in [9] and [10] depend on the assumption that when the input, $x(t)$, can be represented with a sinusoidal, a modified Bessel function can be used to compute an approximation of the DC value for $exp(x(t)/V_t)$, resulting in the peak. Equation 1 is a generalized version of this derivation without any extra assumptions.

Although this detector can be used with alternate tests to predict the peak value of the sensor input, prediction of more complex specifications such as IIP3 or noise figure (NF) demand extra dimensions for the measurement space. Therefore, alternate test mapping functions need at least one other detector. Instead of carefully searching for one, we propose a generic way to generate a class of sensors from a single architecture. Equation 1 is in the form of $V_{o1} = f_1(mean(e^{g_1(input)}))$, where exponential characteristics come from the bipolar transistor. Figure 3 shows the second detector, in which the bipolar devices are replaced with FETs. These two sensors, differential-topology sensors, make use of the same topology but with different active components. In this case, the logarithmic/exponential relation given in Equation 1 is replaced with a square-root/square relation yielding the form $V_{o2} = f_2(mean(g_2(input)^2))$.

Figure 4 shows a generic BIT setup using such sensors: a simple on-chip/package analog signal generator applies the test stimulus to either the DUT or the input sensors through a test multiplexer; the embedded output sensors together with optional input sensors produce DC values to be sampled by the low-cost external tester. These DC values are fed into the specification mapping module in the external tester and non-linear mapping functions output predictions for specifications-under-test.

The accuracy of the *differential-topology sensor architecture* is demonstrated by a series of simulation experiments using a 900 MHz low-noise amplifier (LNA) [11,6] with 5 process variables: the saturation current and the forward gain of the transistors, together with sheet resistance. Each process variable is assumed to have a normal distribution with $3\sigma = nom/10$, where *nom* represents the nominal value for the variable, and σ is the standard deviation. The sample specifications of interest are 1dB compression point (1dBCmp), IIP3, and the NF at the nominal operating frequency and temperature [5,6]. The corresponding alternate test stimulus is selected as a single 900 MHz sinusoid in favor of its simplicity to be generated on-chip/package by a local oscillator or be supplied from a low-end external source.

Two sets of device instances are generated for training and validation purposes using the circuit netlist, device models, and process variable distributions. SpectreRF™ simulator is used to simulate all of these instances at the nominal operating frequency and at the nominal temperature of operation. These simulations are designed to measure actual specifications of interest for each circuit instance by classical methods. Using the measurements and specifications from the training set, a set of non-linear mappings are generated using Multivariate Adaptive Regression Splines (MARS) [12]. Then, these mapping are used with the validation set to check the accuracy of predictions for each specification-under-test.

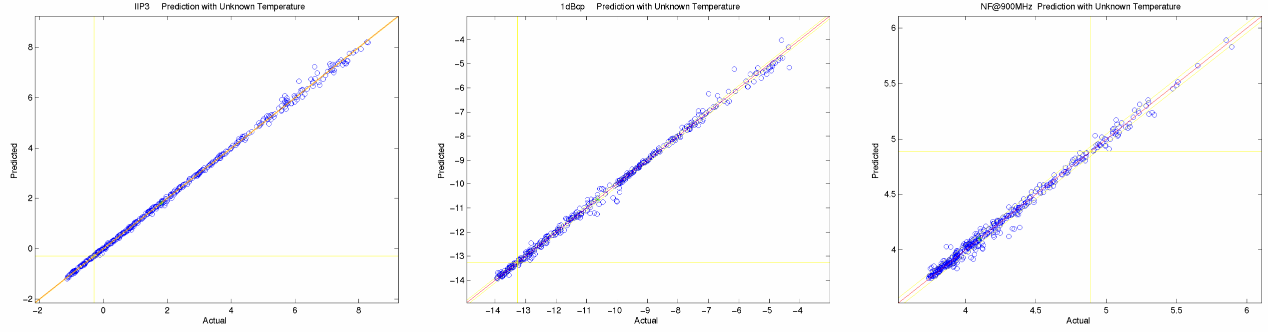

Figure 5: Predicted vs actual specifications for LNA with 2 differential-topology sensors and temperature monitor sensor.

The experiment is designed to be performed in 6 steps, each investigating a controlled branch in the space of possible experiments. The end goal is to demonstrate the auto-calibration ability of differential-topology sensors in the presence of temperature variations by using the two differential-topology sensors at the output of the DUT together with a third sensor at the input. The 1st step checks prediction errors for the LNA, when the DUT analog response samples are used directly to generate the regression models and to predict the specification values of the validation set instead of differential-topology sensor outputs. Although sampling at that frequency is not feasible for a BIT application, these results represent an ideal limit for alternate test predictions without the DC level feature extractors and are listed for comparison. Similarly, the 2nd step uses analog response samples only this time for the validation of the auto-calibration ability. For every auto-calibration experiment, the 100-instance training set is simulated at 6 discrete temperature values -20, 0, 20, 27, 40 and 60˚C; then, a new 400-instance validation set is generated by 4 copies of the original 100-instance validation set. Each instance in this new validation set is simulated at a random temperature in the range [-20 60]˚C. The 3rd step of the experiment implements Figure 4, with the two differential-topology sensors discussed in Section 5 connected only at the output and no input sensors; while 4th step runs the temperature auto-calibration experiment described above with the same setup. The 5th step challenges the ability of the FET-based sensor as an explicit temperature monitor; in this experiment, the simulation temperature is provided to the training set explicitly and MARS mappings are generated for the temperature using this sensor alone. Finally, the 6th step of the experiment validates the proposed auto-calibration methodology by using the FET-based sensor (Fig. 3) at the input together with two differential-topology sensors at the output.

Table 1 shows the summary of results for all 6 steps. For each case, the maximum prediction error is listed as the absolute difference from the original specification. The numbers in Table 1 should always be considered together with secondary measures such as percentage errors and number of misclassifications.

TABLE I. MAXIMUM PREDICTION ERRORS OF THE ACTUAL SPECIFICATION VALUES

#	Temp		IIP3	1dbC	Noise Figure*
1	**No**	**Ideal samp.**	*0.072 dB*	*0.092 dB*	*0.0081*
2	**Yes**	**Ideal samp.**	*3.2 dB*	*4.8 dB*	*1.19*
3	**No**	**2 sensors**	*0.41 dB*	*0.52 dB*	*0.25*
4	**Yes**	**2 sensors**	*3.3 dB*	*4.7 dB*	*1.23*
5	**Yes****	**2+1 sensors**	*3.3 dB*	*4.7 dB*	*1.23*
6	**Yes**	**2+1 sensors**	*0.62 dB*	*0.94 dB*	*0.19*

* at 900 MHz ** Temperature as an explicit property

In order to validate the ability of differential-topology sensors to predict complex specifications, one can compare the results of steps #1 and #3. Both of these experiments are performed at a constant temperature. In the ideal sampled case of #1, the maximum percentage error is 1.1%; whereas in #3 using DC signatures of the differential-topology sensors, the error goes up to 6.2%. Although this error is significantly larger than the ideal one, the accuracy is still comparable to the error resulting from the repeatability of a classical test measurement. Furthermore, the misclassification rate is the same for both setups, only 1 out of 100 instances.

When setups missing the temperature monitor sensor are compared with the corresponding setups performed at constant temperature - #2 vs #1 and #4 vs #3 -, the error percentages are observed to go up significantly, yielding similar misclassification rates around 21%. Although the predictions for the instances simulated at around the nominal temperature are similar in terms of accuracy, the rest of them result in significant deviations from the 45˚ line. This hazy constellation graph is depicted in Figure 6 for IIP3 measurements in setup #4. The figure shows that in the absence of the input sensor acting as a temperature monitor, test results are off-the-chart as expected.

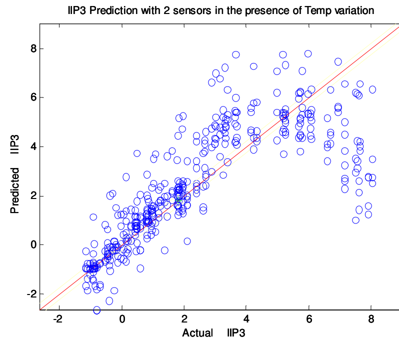

Figure 6: IIP3 Prediction without temperature monitor.

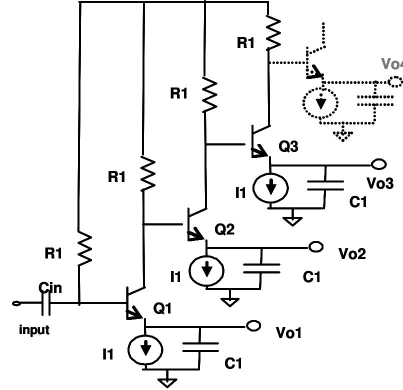

Figure 7: Recursive sensor.

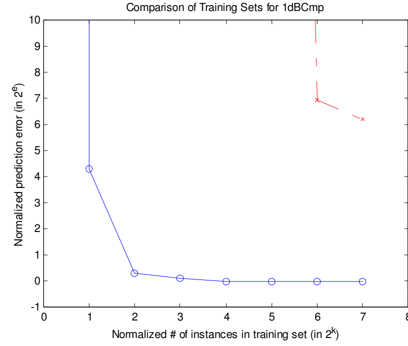

Figure 8: 1dBCmp prediction comparison of training sets with respect to size and use of process monitor.

Steps #5 and #6 are performed in the presence of an input sensor as a temperature monitor. In #5, the signature of this additional sensor is only used for prediction of temperature as an explicit goal; hence, the specification predictions are not different from those in #4. The purpose of step #5 is not to enhance the specification prediction, but to validate the use of the additional sensor as a temperature predictor. The results from the temperature mapping module show that the maximum error is 3.37˚C and the rms error is 1.20˚C. Finally, step #6 validates the proposed auto-calibration methodology. In this case, temperature is treated as an internal variable, and the DC signature of the third (input) sensor is used with the other two output sensors to directly predict specifications-under-test. All three readings are directed to the same mapping function trained to predict IIP3, 1dbCmp and NF. Figure 5 shows the constellation graphs for this setup, where the maximum percentage error is 8.1% and only 3 instances are misclassified out of 400. More constellation graphs about these 6 experiments are presented in [7].

6. Recursive Sensors

The mappings generated by alternate tests are valid under the assumption that the process variations on the manufacturing line are approximately within the same range used for producing the training set. When there is a large shift in one of the process variables, the mappings have to be calibrated accordingly. One can always use a larger training set to account for these process shifts, however the number of instances in the training set grows exponentially with the range of variations. Instead, the input sensors in Figure 4 can be used as process monitors, which can map process shifts efficiently with a small number of training instances.

In order to build process monitors, we first start with the differential-topology sensors and evaluate their potential. Since these sensors are differential, their sensitivity is limited in terms of reflecting large process variations. Each differential-topology sensor makes use of a different active device; for some processes, in which only one type of an active device is present, this will be a disadvantage. Furthermore, each sensor at the output changes the load of the DUT and lumped implementations may require a redesign of the matching network.

Figure 7 shows a variation of the sensor in Figure 2. This new class of detectors is single-ended and the loading is constant regardless of the number of sensors at the output, because each new sensor input is connected to a node of the previous sensor. In this sense, the output function of sensor *m*, is defined recursively in terms of the sensors *1 to m-1* connected between the DUT output and input of the last stage. Furthermore, these sensors require only one type of active device. In this paper we will call *n* such sensors as an nth*-order process monitor* if they are connected at the input of the DUT, and as an nth*-order recursive sensor* if connected at the output. The question of using what combination of process monitors and recursive sensors is a debate between the improvement in accuracy and the extra area overhead, being subject to the magnitude of anticipated process shifts. Although the signatures of different orders are not independent, a certain level of redundancy helps avoid overfitting to noisy signatures.

In order to compare the performance, we ran the same experiment in Table 1, row #3 by replacing the two differential-topology output sensors with a 2nd order recursive sensor. The maximum errors are very similar: 0.46dB, 0.54dB and 0.25 for IIP3, 1dBCmp and NF respectively.

The process shift calibration capability of recursive sensors is demonstrated by a series of simulation experiments using the same LNA in Section 5. In this case, each process variable is assumed to have a normal distribution with $3\sigma = nom/2$, instead of the *nom/10* span. This way the process parameter space is enlarged by $5^5 = 3125$ times, which would require the same order of increase in training set if there were no process monitors. We have designed the experiments by using a 2nd order

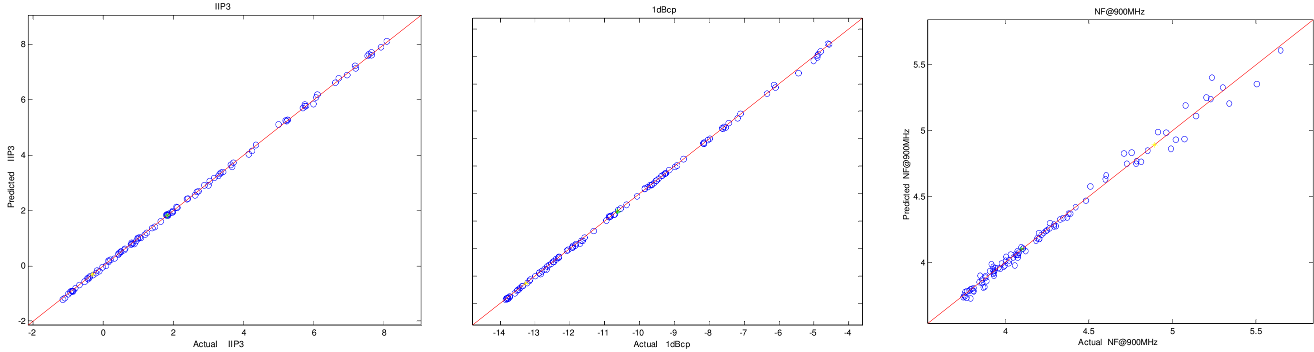

Figure 9: Predicted vs actual specifications for LNA with 2nd order process monitor and 2nd order recursive sensor.

process monitor together with a 2nd order recursive sensor. Although, we have experimented with many other combinations and orders, the accuracy does not increase significantly above the 2x2 configuration. In order to compare the results, we have also run experiments identical except for the absence of the process monitor.

The results of the experiments are depicted in Figure 8. First of all, an experiment with $3\sigma = nom/10$ is conducted with 25 instances in the training set and its results are used as a reference for the experiments with recursive sensor and process monitor. Hence, the x-axis shows the ratio of the number of training samples used with the new sensor set to that of the reference set. Likewise, y-axis shows the ratio of rms error in 1dbCmp prediction. The dashed line in Figure 8 shows that without the process monitors, it is not even possible to generate a mapping with small training sets; even the training set *128* times larger than the reference is off the chart in terms of accuracy. On the other hand, the experiments with process monitors show good tracking at even small set sizes, where *4x* represents a break point. Thus, when a 2nd order process monitor is used with a 2nd order recursive sensor, a training set 4 times larger is adequate to replace the 3125 times larger training set designed for process shifts. The constellation graph for this configuration is given in Figure 9.

7. Conclusion and Future Work

Hardware-based feature extractors provide a promising new platform when used with alternate test methodology. The auto-calibration ability of these sensors is demonstrated with two examples in the presence of environmental variations and large process shifts. The work is currently being extended to even simpler detector structures that can serve as process variation monitors.

Acknowledgment

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