Alternate Test of RF Mixers by Current Signatures

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***Abstract* — This paper describes an alternate test methodology for radio-frequency mixers. The methodology is based on current signatures obtained by sampling the filtered supply current when the circuit-under-test is stimulated by a single tone sinusoidal. Sampling of supply current instead of voltage eliminates the parasitics and loading due to test circuitry on the signal path, hence provides a non-invasive built-in-self-test methodology. Furthermore, the experiments show that specification prediction accuracy is not significantly degraded by decreasing the stimulus power. The goal of the paper is to examine the advantages and disadvantages of current-based alternate tests and provide feasibility analysis for future directions.**

***Index Terms* — Built-in testing, current measurement, integrated circuit testing, mixers, testing.**

I. Introduction

The last decade witnessed an ever-increasing test challenge for analog and radio-frequency (RF) circuits. While the design community has pushed the design envelope far into the future, the test barriers have not kept pace with the test requirements of high speed, integrated wireless and wired communications designs. High speed mixed-signal testers above 2 GHz are prohibitively expensive and they are still one generation behind the integrated circuits to be tested. Furthermore, in contrast to digital systems, analog/RF components have only a few input/output nodes, limiting the access to internal points. Probing of these nodes threatens the signal integrity and may cause severe impact on device performance.

In order to reduce tester costs and limit the test bandwidth requirements, there is a trend to move tester functionality to the close proximity of the device under test (DUT) in the form of built-in test (BIT) and built-off test (BOT). BOT migrates high-speed functions of the automatic test equipment (ATE) to the tester load board, while BIT implements these functions within the same chip or package. Generally, all high speed features necessary to test different specifications under test can not be practically implemented on the load board or on-chip. Therefore, BOT/BIT is likely to make use of alternate test methodology, which replaces a number of ordinary tests with a single test performed by less number of resources. Alternate tests are designed such that the response signature of the DUT is highly correlated to the specifications under test in the presence of process variations. Other than simple pass/fail decisions, the test results can also be in the form of quantitative specification value predictions so as to provide a measure for the quality of each prediction.

The parasitics associated with test electronics constitute one of the major problems for BIT of RF components, which are carefully designed for matched loads and cannot tolerate additional losses associated with the test multiplexing and coupling circuitry. These negative effects have to be compensated at the design phase of the DUT, or there is a severe impact on the device performance. Monitoring supply current proposes a non-invasive alternative to these kinds of problems. Since the observation node is not on the critical signal path, supply current can be copied and monitored without significant degradation of circuit performance.

Another challenge for BIT/BOT is stimulus generation: the on-chip/board features may be limited in frequency and power. One solution for frequency is making use of an external low-frequency test input and upconverting it to the RF range using built-in/off electronics. Alternatively, one can use lower frequency signals to stimulate the DUT and sample the response to predict specifications at the operating frequency. Such a mapping is inherent to the alternate test process. On the other hand, accuracy of the voltage sampling based specification prediction heavily depends on the stimulus power. In some cases, the correlation between the specifications and response signatures are strong only when the stimulus has high power levels. This is especially true when the specification-under-test involves nonlinear characteristics apparent through power compression. However, the on-chip/board resources may not be adequate to supply such large power levels. In this paper, our experiments show that the specification prediction accuracy is not significantly degraded by decreasing stimulus power when the response signature is generated from the supply current as opposed to output voltage.

In this paper, we examine the advantages and disadvantages of current-based applications of alternate

tests in Section 3. Section 4 describes the details of the methodology. The experiment presented in Section 5 provides a preliminary feasibility study for using current signatures with alternate tests. Finally, Section 6 suggests future directions for supply-current-based alternate tests.

II. Background

Advantages of alternate tests has been demonstrated in specification-based testing and fault diagnosis of analog circuits [1-2]. Built-in applications and integration feasibility of the methodology is featured in [3-5]. Lately, extensions of this methodology are employed to test critical specifications of RF components [6-7]. One recent paper by Srinivasan et. al. [8] samples the supply current of a power amplifier and uses an alternate test stimulus as the control voltage to the amplifier.

Supply current based testing has extensive applications in digital systems. Iddq testing provides a powerful and cheap tool for wafer level testing of digital systems built of MOSFETs, and its extensions have the potential to eliminate burn-in test [9]. Although submicron devices proposed a challenge with increasing leakage currents, variations of Iddq, such as delta Iddq, enhance the resolution [10] partially eliminating the problem. A generalized theory of current signature analysis and its extension to transient supply current monitoring is described in [11]. Finally, [12] presents a built-in architecture for on line monitoring of quiescent and transient supply currents, while [13] demonstrates a similar built-in implementation for analog structures.

III. Current Signatures in RF Testing

Although the use of current signatures proposes advantages as discussed in Section 1, it also suffers from disadvantages specific to RF testing. The main advantages of using current signatures can be summarized as follows:

- Non-invasive: Tapping supply current has little impact on circuit performance when compared to sampling the output voltage response.
- More observable: Different branches of supply currents can be isolated and individually sampled to reveal faults in different stages, which may otherwise be masked by following stages of the circuit.
- BIT friendly: Predictions from supply current exhibit high correlation to specifications-under-test even for small power levels of the input stimulus.

On the other hand, using supply currents for BIT of RF devices have the following drawbacks:

- BIT area overhead: Current mirrors, current-to-voltage converters, ADCs and current filters may populate complex structures when compared to the RF DUT. However, for complex systems like systems-on-chips and systems-on-packages, this overhead can be reduced by modularity, component reuse and test scheduling.
- Signature Resolution: For RF components relying heavily on bias currents, the supply current may be dominated by the bias component and the variation due to soft faults may be below the signature resolution. This is especially valid for low-noise amplifiers (LNAs) made of BJT devices. Our experiments on such a LNA suggest that the variation in signatures is below 0.1% of the bias current.
- Power consumption: For BIT solutions with current mirrors, the supply current is copied and sampled in order not to violate the normal operation regime of the DUT. This extra current will double power consumption and threaten the reliability of high power devices such as power amplifiers.

IV. Methodology

In the proposed methodology, the DUT is excited by an alternate test stimulus. Various test stimulus generation algorithms are presented in the literature [1,2,6,7], the proper implementation depends on both the structure of the device and the specifications-under-test. After the circuit is stabilized, the supply current is monitored. For BIT applications, this stage consists of a current mirror followed by a simple current-to-voltage converter. The key criterion for the monitoring circuit is minimization of the effects on DUT operation, while the accuracy of the monitor is a secondary target. Although state-of-the-art monitors such as [9, 11-13] can be used, the non-linearity of the current-to-voltage transfer function is not critical since these effects can be implicitly handled by the prediction mapping. Then, the monitored current is filtered and sampled into a digital signature. These signatures are fed into the specification mapping functions producing the predictions for each specification-under-test. Later, these specification predictions can be compared with pass/fail thresholds to mark the DUT as good or bad.

The specification mapping functions are generated by the alternate test methodology. The variation of any process parameter in space P affects the circuit specification S by a corresponding sensitivity factor. If M is the space of measurements made on the DUT, the variation in the parameters also affects the measurement data in the measurement space M of the circuit by a

corresponding sensitivity factor. Given the parameter space P, a mapping function $f: M \rightarrow S$ can be constructed for the circuit specifications S from all the measurements in the measurement space M using nonlinear statistical multivariate regression. In our methodology, these specification prediction mappings are constructed with multivariate adaptive regression splines (MARS) [14] by using a number of training instances. These instances are generated by Monte Carlo simulations over process variations. The actual specification values of the training set are measured using standard "datasheet" tests.

V. Case Study: Radio-Frequency Mixer

The proposed methodology is demonstrated on a RF downconversion mixer. Figure 1 shows the schematic of the 920 MHz mixer with 1GHz local oscillator. The saturation currents and forward gains of two different kinds of transistors, together with the sheet resistance are considered as process variations. 150 Monte Carlo instances are generated for the training set, and 50 independent instances are used to validate the mapping. Although the output of a downconversion mixer does not exhibit significant frequency components above the downconversion frequency (80MHz in this case), its supply current reflects the effects of local oscillator (1GHz) and has much more complex frequency characteristics. In this form, the current waveform presents a rich signature and produces very accurate mappings. However, in order to be able to compare its performance with that of voltage based mapping, two waveforms have to be sampled at the same rate. This process requires an analog lowpass filter before the sampling. For the sake of simulation time, the filter is created in digital domain using Matlab. The analog filtering process is simulated by sampling the Spectre transient output at a very high frequency that can represent a realistic digital counterpart of the original supply current, and then by filtering in the digital domain. Many filters with different properties have been examined, and it is concluded that the filter type has a minor effect on the final accuracy of the predictions. Figure 2 shows the frequency response of the 4th order Type II Chebyshev filter that is used to generate the results presented in this paper. The filtered waveform is sampled at 320MHz and the results are converted to 6 bit accuracy.

Table 1 shows the prediction accuracies for 4 specifications: input referred third order intercept point (IIP3), 1 dB compression point (1dBCp), conversion gain at 920MHz (CG), and power supply rejection ratio at 920MHz (PSRR). The first two rows list voltage and current-based prediction errors for an input power of -5dbm. The maximum error for voltage-based prediction is below 0.5% while that of current is below 1%. The third and fourth rows list the same predictions with an input power of -30dbm. In this case, voltage-based prediction error is more than 2.5%, while the current-based prediction stays almost constant below 1%. Figure 3 shows the predicted versus actual specification values for the current-based test with -30dbm input.

VI. Future Directions and Conclusion

This paper presents a feasibility study for using current signatures in specification-based alternate tests of RF components. The example, RF downconversion mixer, is simulated by Spectre and the sampled data is filtered in Matlab by a digital filter. A detailed study has to be conducted to investigate the loading effects of an analog current mirror and filter at the transistor level. Although the mapping considers 1% measurement noise and 6 bit accuracy in filtered current signatures, the non-ideal effects of monitoring circuit and analog-to-digital converter are yet to be studied.

As a conclusion, the alternate test of RF mixers by current signatures demonstrates a non-invasive alternative to voltage based built-in tests. The methodology can be employed when the overhead of additional filter and current converters are not significant compared to the value added by current sampling.

Acknowledgement

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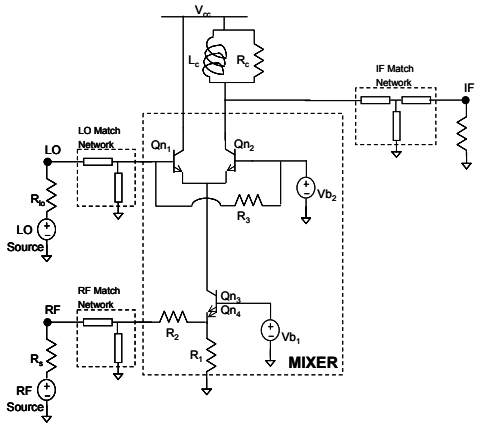

Fig. 1. Schematic of the 920MHz low-power communication mixer.

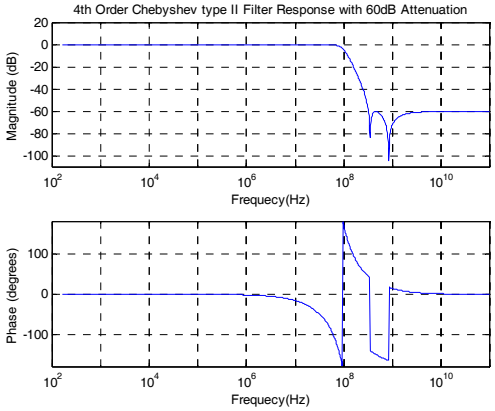

Fig. 2. Frequency and phase response of the filter.

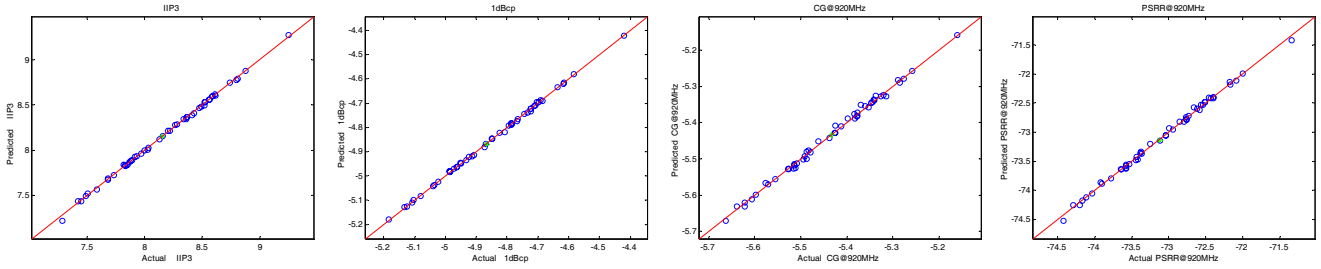

Fig. 3. Actual vs prediction values for specifications of the mixer.

TABLE I
MAXIMUM % ERROR IN PREDICTION: COMPARISON FOR CURRENT VS VOLTAGE AT -5DBM AND -30DBM

Type	Input (dbm)	IIP3	1dbCp	CG	PSRR
Voltage	-5	0.448	0.196	0.042	0.017
Current	-5	0.807	0.218	0.324	0.104
Voltage	-30	2.660	0.258	0.078	0.035
Current	-30	0.885	0.230	0.343	0.128