Feature Extraction Based Built-In Alternate Test of RF Components Using a Noise Reference

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Abstract—**This paper addresses the cost, signal integrity and I/O bandwidth problems in radio-frequency testing by proposing a feature extraction based built-in alternate test scheme. The scheme is suitable for built-in self-test of radio-frequency components embedded in a system with available digital signal processing resources, and can also be extended to implement built-in test solutions for individual RF devices that have access to a low-end digital tester. The process applies an alternate test and automatically extracts features from the component response to predict specifications like third order intercept point, 1dB compression point, noise figure, gain and power supply rejection ratio. The proposed scheme makes use of low-speed low-resolution undersampling to eliminate the need for a bulky analog-to-digital converter and the use of a noise reference for comparison makes it possible to compensate for imperfect stimulus generation. The simulation results for a 1 GHz downconversion mixer and a 900 MHz low-noise amplifier present an average of 97.3% prediction accuracy of specifications under test.**

I.   INTRODUCTION

Mixed-signal electronics has come a long way with heavy use of radio-frequency (RF) components in telecommunication systems. System-on-a-chip (SoC) and system-on-a-package (SOP) structures with digital processors and multi-gigahertz RF components propose great challenges in terms of electrical testing. In contrast to the test of digital systems, the analog parts of such structures have only a few inputs and outputs and probing these nodes for test purposes threatens signal integrity when one considers the carefully matched no-loss tolerant RF interconnects. Even when such coupling is affordable, the test designer faces problems in relaying the multi-gigahertz internal signals through I/O channels to the external tester, because these channels are bounded by the bandwidth of low-frequency end-to-end signals they are originally designed for. In other words, the rate of increase in bandwidth of the internal RF paths exceeds the rate of increase in bandwidth of the mixed-signal core I/O channels [1].

Another significant bottleneck results from external tester costs. Production testers with RF capabilities supporting frequencies above 2 GHz are prohibitively expensive in the multi-million dollar range. For mixed-signal circuits, test can be a limiting factor contributing up to 50% of the manufacturing cost [2]; introduction of RF components increases this percentage, when it is possible to find such high-frequency testers at all. Furthermore, the mixed-signal and RF testing practices lack a systematic approach similar to the IEEE

boundary scan standard for digital cores [3]. Although such standards are extended to mixed-signal systems [4], the practical problems of analog test stimulus generation and response acquisition are yet to be solved contributing a significant amount of research in analog testing [5-8]. The current ad-hoc approach to analog testing is provided on a per circuit basis [9] and introduces significant overhead to the test development time, hence stresses the cost associated to time-to-market extensions.

All these problems are due to an imbalance between the development of new design paradigms and corresponding test practices. While the design community had pushed the design envelope far into the future, the test barriers have not kept pace with the test requirements of high speed, integrated wireless and wired communication systems. In this sense, built-in test (BIT) proposes a flexible paradigm for production test of such systems while providing scalability with advances in design. BIT includes designing test hardware on-chip, supporting the test hardware with design for testability (DfT) features and designing in standard communication protocols that allow an external tester to control the test procedure with low-bandwidth access and hence, lower cost external testers. In specific cases –such as SoC with on chip digital signal processing (DSP)- almost all the test functions can be performed on-chip, transforming the BIT into autonomous built-in self-test (BIST) with little or no external tester control. The use of BIST in digital systems has been implemented as an integral part of the design flow in many industrial practices as an effort to overcome the time-to-market pressures. Analog/RF BIST will play an identical and essential role once few barriers have been overcome. In this way, the distinction between the circuit designer and the test engineer will disappear favoring a DfT approach to yield higher fault coverage and less signal integrity problems.

In this paper, we propose a BIST scheme for RF components embedded in a system with available DSP resources. This scheme addresses the precise analog signal generation and response acquisition problems associated with previous analog BIST approaches. The automatic extraction of test response features from the component-under-test (CUT) response makes the scheme favorable for DfT flow. The CUT is excited by an embedded oscillator, and a one-bit noise-referenced comparator captures the response. The resultant bit stream is fed into the digital scan chain of the system and recollected at the DSP resources, which reconstructs an approximation of the original spectral response. Further algorithms extract features from this spectrum, and they are

mapped into predictions for RF specifications under test. The mapping makes use of alternate test principles. The two key features of the proposed approach are: (1) compensation for imperfect stimulus and (2) use of a low-speed low-resolution noise-referenced comparator for sampling. These two features make the proposed scheme ideal for low-cost and low-area overhead BIST implementations. Note that the second aspect above was first proposed by Negreiros, Carro and Susin [14]. However, while [14] presents a generic approach to noise-referenced fault detection, no bridge to traditional specification-based analog/RF testing was developed. Fault-based testing has its own caveats, namely the lack of "accepted" fault models and failure mechanisms. For the technique of [14] to succeed, it is desirable to port it to the area of specification-based testing which is essentially *fault-independent*. In other words, it should be possible to infer the analog/RF specifications of the CUT directly from the test response. Such a step is not possible without proper *response feature extraction* as discussed in this paper. It is shown that once such feature extraction is performed, it is possible to determine all the CUT specifications from the observed digital test response very accurately. In addition to that, the generation of the proposed BIST plan is fully automated; hence it can be integrated to the design flow as a designer-friendly DfT step. The methodology can also be extended to implement BIT schemes for systems that lack the power of DSP resources, but instead have access to a low-cost low-speed digital tester.

The rest of this paper is organized as follows: Section 2 gives a summary of the background on BIST of analog components and mixed-signal systems. Section 3 discusses the proposed methodology while Section 4 explains the test architecture. Finally, Section 5 presents simulation results for two implementations of the scheme.

II. BACKGROUND

Built-in test of digital systems have been a common practice for the last two decades, and most of the time offers the only feasible approach when system complexity is in the order of modern microprocessors. Many major companies have adopted the available IEEE standard [3] to implement a BIST scheme and made the practice a de-facto standard in their design flow. The extension of this standard is available for mixed-signal systems [4]. Although the standard offers ways to address accessibility issues in mixed-signal systems, the analog test stimulus generation and response acquisition still remains an open problem.

A second BIT paradigm uses analog-to-digital (ADC) and digital-to-analog (DAC) converters to address these open problems. In these schemes, the analog test stimuli are generated by DACs using bit streams, and the response is quantized by ADCs to propagate in digital form [10, 11]. These solutions require powerful ADCs and DACs in the system, which may be not be feasible in terms of area-overhead when they are not already built-in. Even when they are available in the system, the BIT interconnections introduce performance degradation in normal operation of these components, which is usually not tolerable for the system designer. These interconnection problems are vitally significant when very high-speed RF paths are present in the system.

Alternatives to the two paradigms propose new BIT techniques for systems with analog and RF components. The loopback techniques in [12] and [13] make use of the "duality" present in the transceiver systems. The output of a receiver is analyzed by its dual transmitter and vice versa. However, test interconnections require additional components to balance power levels and to overlap the frequency bands of two subsystems. Furthermore, consecutive stages mask fault effects, hence testing is possible only at a system level making diagnosis a hard problem. Another approach modifies each component to introduce loops and oscillate by itself [8]. The applications of this approach are yet limited to specific components where stability conditions can be satisfied.

As discussed before, [14] introduces an approach where the response acquisition is carried out by a simple analog comparator. It is shown that the parametric and catastrophic faults can be detected by comparing the signal with pseudorandom noise and using spectral properties maintained after comparison. Finally, two recent approaches implement vehicles to ease BIST generation; [15] introduces a methodology to build on-chip spectrum analyzers and [16] describes a Vernier undersampling scheme to address response acquisition of very high speed components.

III. PROPOSED TEST METHODOLOGY

The classical production testing approach to specification based analysis makes use of a large set of functional tests that add significantly to the test time and final cost of the integrated circuit. On the other hand, fault based testing provides an inexpensive alternative to functional tests, but it usually fails to consider the parametric fault effects and the results may not have a direct significance in terms of data sheet specifications. Specification-based alternate tests propose a way to bridge the gap between these two methodologies. In this scheme, the data sheet specifications of a CUT are predicted by analyzing its response to a specific input pattern. The CUT response can be considered as a signature for the effects of process variations specific to the CUT instance. These process variations also make the specification values derive from their ideal values. Figure 1 depicts this relationship.

In this paper, we propose a methodology to extend specification-based alternate tests in a way to accomplish low-cost built-in self-test of RF components. The methodology follows the theory in [17], but proposes a novel way to extract features from response signatures. Previous work uses samples of the signature directly, but that approach experiences limitations in terms of sampling speed and timing accuracy when applied to very high-speed RF components [18]. The use of indirect features relaxes the constraints on sampling and accuracy, hence implements a method suitable for BIST applications. Monte Carlo simulations are utilized with nonlinear regression analysis [19] to generate mappings from these features to each specification value. In some cases, a model calibration phase as discussed in [17] may still be necessary to account for the differences between simulation models and hardware realizations or when process shifts are present on the production line.

The sampling of the signature is a critical part of the alternate test such that the speed and accuracy of sampling mostly defines the accuracy of predictions. For RF components operating in the gigahertz range, this requirement
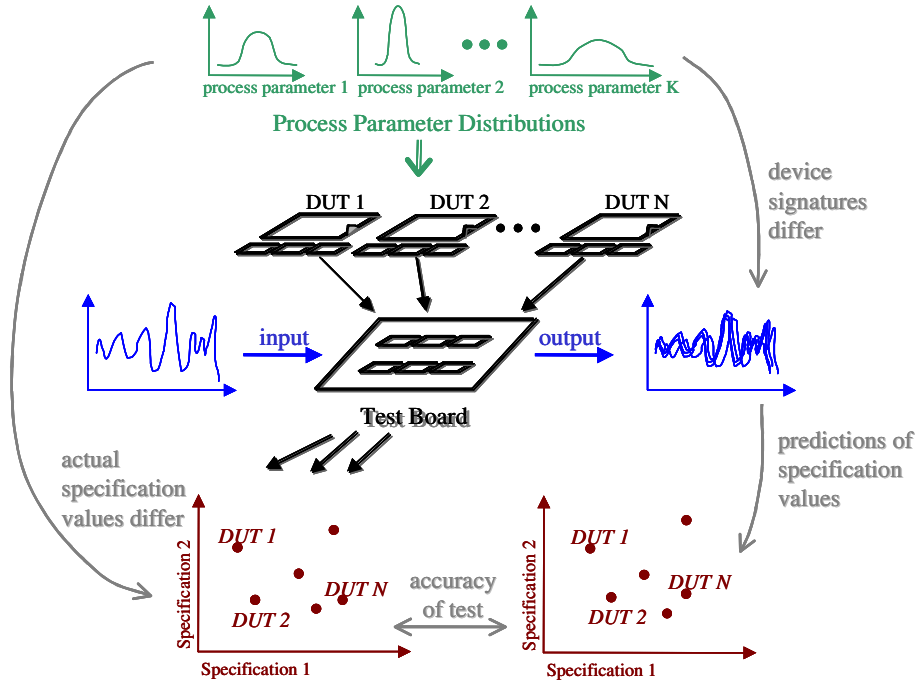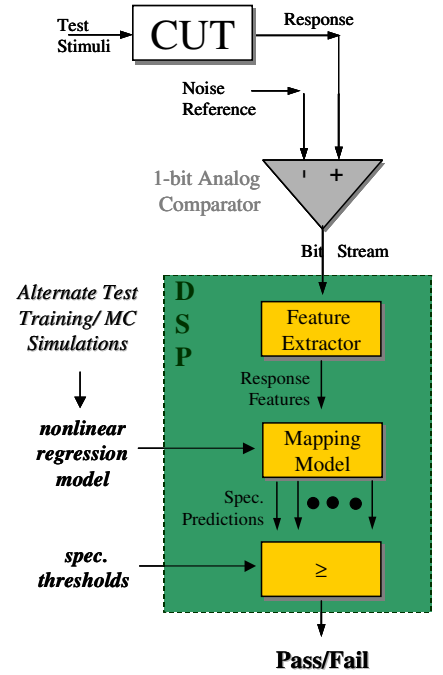
Figure 1:   Alternate test methodology.

Figure 2: Noise-referenced alternate test.

defines a problem, since the nyquist sample rate of such signals and their harmonics may far exceed the capabilities of ADCs already present on-system. Even if such ADCs are present on-system, they introduce significant area overhead and signal degradation when interconnected as a part of the BIST scheme. In [14], a low-cost sampler with low area overhead is introduced. In this scheme, the signal is compared with noise to generate one bit output such that the power spectral density (PSD) of the resultant bit stream can be processed to differentiate between fault free and faulty circuits. The comparison process can be modeled as a hard-limiter and when the input $x(t)$ is a stationary process with zero-mean, the autocorrelation of the output $y(t)$ is given by [20]:

$$R_y(\tau) = \frac{2}{\pi} \cdot \arcsin(\frac{R_x(\tau)}{R_x(0)}) \tag{1}$$

Equation 1 states that the statistics of the input will be preserved at the output of a hard limiter. When $x(t)$ is compared with white noise, the resultant autocorrelation will be a scaled (by eq. 1) and biased form of the original. The level of bias depends on the amplitude of white noise [21], which must be greater than or equal to the amplitude of signal to be compared. Finally, the result will also be transformed by the arcsine function. Under reasonable conditions, the nonlinear regression mapping can trespass the effects of all three operations. From a practical point of view, the noise comparison process is analogous to a random sampling of the signal; hence, as the above discussion suggests, the spectral content at the output of the comparator is identical to a scaled version of the original plus some noise floor resulting from random sampling. Main spectral components of this signal may still be above the noise floor, and carry valuable

information about the original signature. In this paper, we implement a feature extractor, which performs a fast fourier transform (FFT) operation and then automatically detects spectral components above the noise floor introduced by the noise reference.

The feature extractor is based on wavelet transformations. Coiflets of the second order [22] are used to decompose the original spectrum (s) into 8 levels of coefficients, and then some of the coefficients are eliminated using a soft minimax de-noising method [23]. The signal is reconstructed by the remaining coefficients resulting in the de-noised signal (Ds). The residual (Rs):

$$Rs(f) = Ds(f) - s(f) \tag{2}$$

defines the frequency dependent noise floor. After applying a guard band above this level, all the spectral components below this floor are removed. The remaining spectral components define the final features extracted for mapping. In the proposed methodology, a set of training examples are simulated with process variations given by process parameter distributions. These Monte Carlo (MC) simulations define the feature extractor parameters and the mapping between these features and specification values. Figure 2 depicts the overall testing process: the response signature is compared with the noise reference and one bit of data is generated at a time. A large number of these bits are recollected at the feature extractor and the spectral results are trimmed accordingly after the FFT. The few resultant spectral elements are fed into the mapping model to generate predictions for specifications under test. These specifications are compared with hard-coded threshold values and the test process displays a final bit representing either pass or fail. The DSP components of this process are summarized

x, xmc	: comparator output, digital bit stream
X, XMC	: reconstructed FFT
w	: vector of wavelet transform parameters
s	: vector of DUT specifications
nf_i	: FFT noise floor for i^{th} training instance
FE	: set of extracted frequency indexes
f	: vector of extracted features
M_j	: nonlinear regression model for j^{th} specification
t	: vector specification thresholds
D	: digital scan chain
p_i	: pass-fail decision for i^{th} specification
n_s	: number of specifications
n_{mc}	: number of Monte Carlo instances
P	: pass/fail decision for DUT

// generate feature extractors
FE $\Leftarrow U$
for $i = 1$ to n_{mc} **do**
    xmc_i $\Leftarrow$ *SimulateMonteCarloInstance(i)*
    $XMC_i \Leftarrow$ *ComputeFFT(xmc_i)*
    nf_i $\Leftarrow$ *ComputeFFTNoiseFloor(XMC_i, w)*
    FE $\Leftarrow FE \cap j$, *for* $j = Index(XMC_i > nf_i)$
end for
// algorithms for DUT
x $\Leftarrow$ *CollectBitStreamfromScanChain(D)*
X $\Leftarrow$ *ComputeFFT(x)*
f $\Leftarrow X_j$, *for* $j \in FE$
for $j = 1$ to n_s **do**
    s_j $\Leftarrow$ *ComputeMapping(M_j, f)*
    p_j $\Leftarrow$ *ApplyGo/No-GoThreshold(s_j, t_j)*
    P $\Leftarrow P$ & p_j
end for
return *P*

Figure 3: Algorithm for pass/fail calculation using DSP resources.

Figure 4: The proposed test architecture for a RF component embedded in a system with DSP resources.

in Figure 3 together with the algorithm to generate feature extractor parameters.

IV. PROPOSED TEST ARCHITECTURE

Figure 4 shows the proposed test architecture for a RF component embedded in a system with DSP resources. Such test cases are common in highly integrated systems like system-on-a-chip (SoC) and system-on-a-package (SOP) applications. Most of the time, these implementations already include support for boundary scan test of digital components. The proposed architecture makes use of this digital scan chain to capture the output of the comparator and to feed it into the available DSP resources. The algorithms depicted in Figure 3 can be implemented in these resources, which may be available in the form of FPGAs, ASICs or general purpose processors.

The additional BIST components consist of an analog multiplexer or switch, an oscillator with relaxed constraints on precision, a low-speed one-bit analog comparator, and a pseudo-random noise generator. The oscillator supplies the analog stimulus for the CUT. It is tuned to a predetermined frequency and the linearity constraints are relaxed in the sense that the imperfections in the stimulus can be compensated by the methodology. Hence, it is not a critical design component and does not require a significant design effort if implemented in a DfT flow.
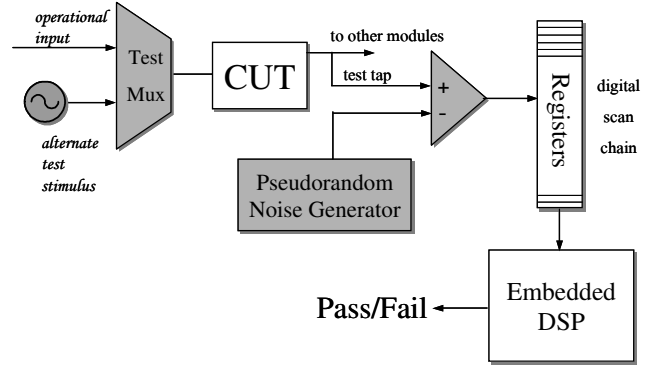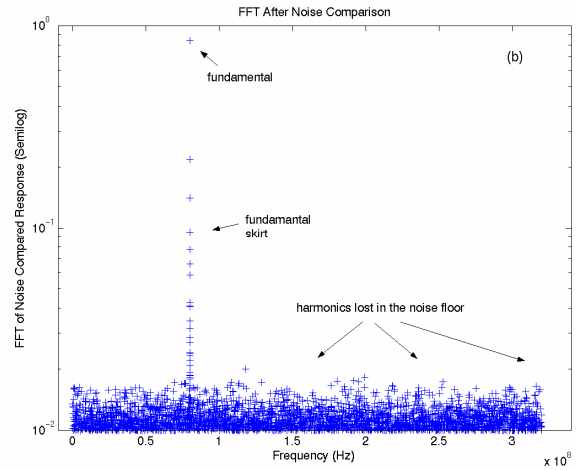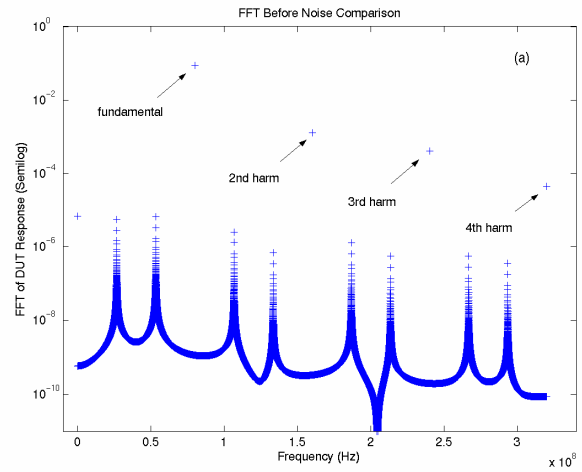

Figure 5: FFT of the output response before (a) and after (b) noise comparison.

The pseudo-random noise generator makes use of a simple RC circuit and a LFSR to generate analog noise with specifications discussed in Section 3. This analog noise is fed into the one-bit analog comparator, which operates at a frequency one order below the necessary nyquist rate. An averaging circuit can be employed instead of a sample-and-hold to relax the constraints on the design of the comparator. It compares the analog noise with the response of the CUT, and generates a one-bit digital output. Proper sampling is possible thanks to undersampling, which makes use of the almost periodic nature of the CUT response.

The single bits at the output of the comparator do not carry information one-by-one, but when the sampling is carried over many cycles the resultant bit stream has an approximate imprint of the spectral content of the CUT response. This process is analogous to sampling the CUT response at random intervals and then extracting stochastic parameters from those samples. When the FFT is constructed at the DSP resources, the effect of random sampling dictates itself as a noise floor. Figure 5 shows the FFT semilog plot of a CUT response before and after the noise-based comparison process. As one can observe, the higher order harmonics present in the original response are lost in the noise floor, while the fundamental harmonic is still visible with a skirt around it. In an ideal undersampling process, this skirt, which is visible after the noise-based comparison in Figure 5, would not be present and the FFT would consist of a single amplitude value around each harmonic. In practice, the effects of accuracy problems in the sampling interval and in the sampling jitter dictate a skirt around the harmonics. From a different point of view, this skirt is a translation of the phase information in the transient signal to amplitude information in the FFT. Thanks to this translation process, alternate tests can use the amplitude information in the skirts to more accurately predict specifications under test. The wavelet based automatic noise floor detection algorithm chops of the amplitudes below noise floor level, but the skirt amplitudes above this level are preserved and fed into the alternate test model for mapping into specification predictions.

A variation of this BIST architecture can be implemented as a BIT scheme for RF components without proper DSP support. The oscillator, pseudo-random noise generator and the comparator are still embedded with the DUT, but the digital output of the comparator is latched and transferred to an external digital tester via a low-speed link. In this case, the feature extraction and mapping are implemented in the tester. This variation proposes a very-low cost alternative to high-speed RF testers.

V. SIMULATION EXAMPLES

In this section, we demonstrate and validate the proposed architecture by two simulation examples.

The first example is a 1 GHz downconversion mixer. The corresponding alternate test stimulus is a 920 MHz sinusoid accompanied by a 1 GHz local oscillator (LO) signal. The 80 MHz response is undersampled at 71.1 MHz to generate 65536 samples of an effectively 640 MHz signal –nyquist rate of the 4th harmonic-. The feature extraction algorithm removes the spectrum of the 2nd, 3rd and 4th order harmonics since they are below the noise floor. As a result, the only extracted feature is 11 samples of the skirt around the fundamental harmonic. These samples are fed into a regression model generated by

TABLE I.   MAXIMUM PREDICTION ERRORS IN PERCENTAGES OF THE ACTUAL SPECIFICATION VALUES

		IIP3	1dbC	Gain*	PSRR*
1	**Mixer Ideal**	1.21%	1.02%	0.454%	0.112%
2	**Mixer BIST**	2.90%	1.56%	1.14%	0.365%
3	**Mixer BIST with noise in stimulus**	7.07%	4.46%	2.68%	1.10%

* at 920 MHz

		IIP3	1dbC	Noise Figure**
4	**LNA Ideal**	1.1%	1.02%	0.0190%
5	**LNA BIST**	8.96%	2.38%	0.799%
6	**LNA BIST with noise in stimulus**	13.04%	5.60%	1.31%

** at 900 Mhz

150 MC instances of the mixer netlist. The accuracy of the final test plan is validated by a separate set of MC instances that are generated independently from the training set. Figure 6 shows the predicted versus actual specifications of 50 MC instances in this validation set. The maximum prediction error is 2.9% for the IIP3 specification. As one can observe, the IIP3 specification is predicted accurately from only the information on the fundamental harmonic. The maximum prediction errors for the other three specifications are listed in the 2nd row of Table 1. Performing go/no-go tests on these specifications and their corresponding threshold values show that all 50 instances are classified as they should be. The 1st row of Table 1 also lists prediction errors for the same mixer under identical conditions, but this time the CUT analog response samples are used directly to generate the regression models and to predict the specification values of the validation set. These results represent an ideal limit for alternate test predictions without the noise reference and listed for comparison.

The second example is a 900 MHz low-noise amplifier (LNA). The corresponding alternate test stimulus is a 900 MHz sinusoid. The response is undersampled at 89.1 MHz to generate 65536 samples of an effectively 7.2 GHz signal. The higher order harmonics are again eliminated by the feature extraction algorithm, feeding 10 samples of the skirt around fundamental. The regression model is generated by 150 MC instances and specifications are validated using a separate set of 50. Figure 7 shows the predicted versus actual specification values for these validation instances. The maximum prediction error is 8.96% for the IIP3 specification. The corresponding maximum errors for other two specs are listed in the 5th row of Table 1. Only one good instance is classified as bad after the go/no-go thresholding. The ideal alternate test prediction limits are also listed in the 4th row of Table 1.

Further experiments are conducted to validate the compensation in the presence of imperfect stimulus generation. In these experiments, the ideal sinusoidal is superposed with random noise, which has an amplitude variation swing equal to 10% the swing of ideal sinusoidal. The regression models and feature extractors generated by the ideal sinusoids are used for predicting specifications of the validation sets stimulated by imperfect sinusoids. For both the mixer and the LNA, the predicted specifications follow the actual ones with a small offset. The maximum prediction errors are 7.07% in IIP3 for the mixer and 13.04% in IIP3 for the LNA. The 3rd and 6th rows in Table 1 list other maximum errors for the mixer and LNA under imperfect stimulus.
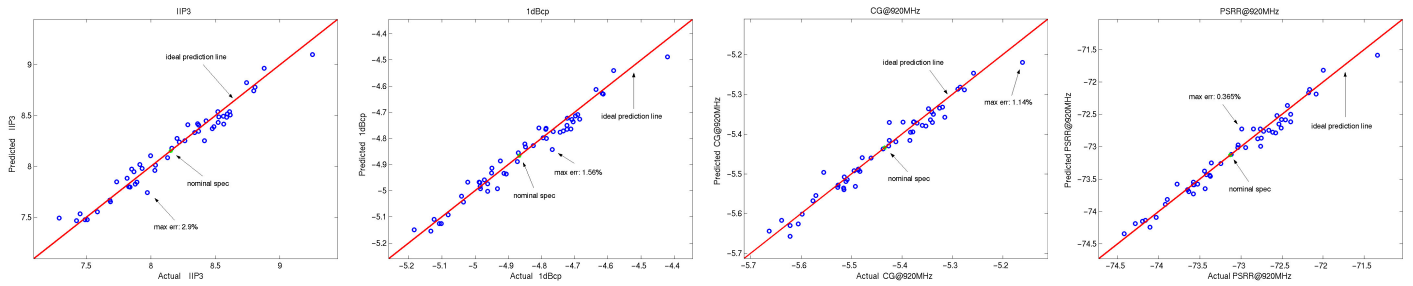
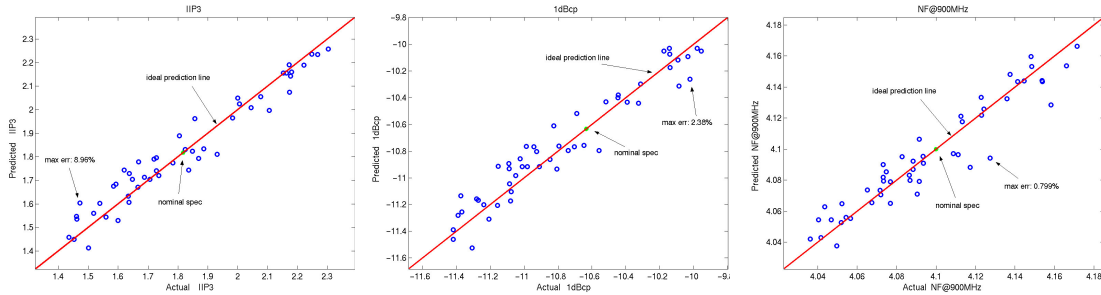Figure 6:   Predicted specification values for 1 GHz downconverter.

Figure 7:   Predicted specification values for 900 MHz LNA.

VI.   CONCLUSION

In this paper, we have proposed a low-cost BIST scheme for RF components embedded in a system with digital signal processors. The methodology predicts complex specifications quantitatively by the use of alternate tests on spectral features generated by DSP algorithms. The BIST generation process is fully automated, hence proposes a designer-friendly DfT scheme. We have also proposed a way to extend this scheme to BIT of RF devices with low-cost digital testers. The methodology is verified by two simulation examples that present close tracking of all the specifications even in the presence of imperfect stimuli. We are currently working on hardware validation of the experiments.

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